


Quanta Project Name: GM7B

Dell Project Name: Shatner

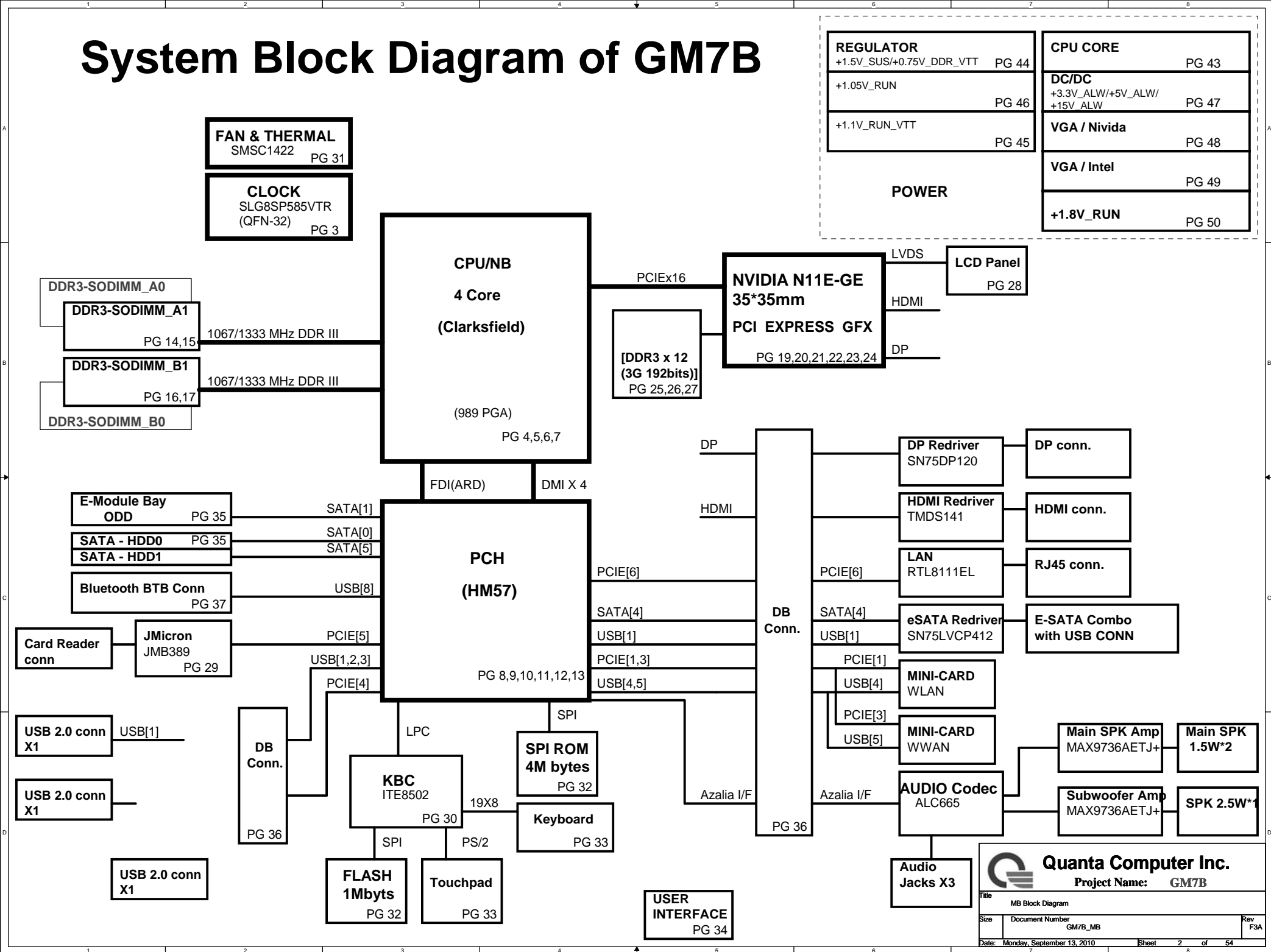
A00(QT) Stage

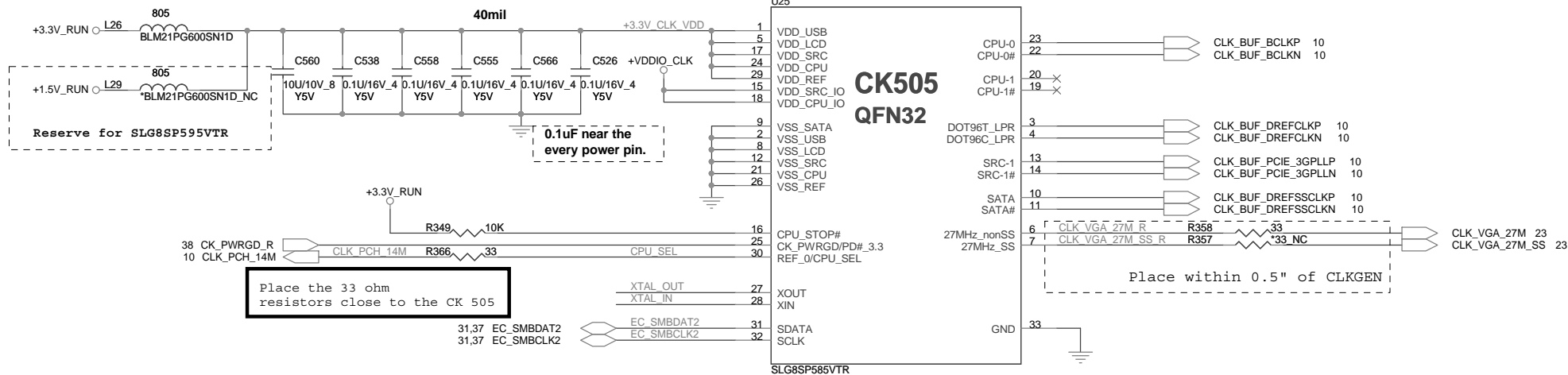
BOARD REV : F

2010-08

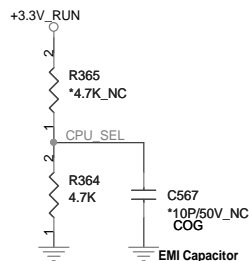
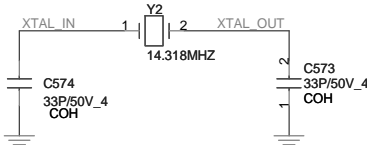
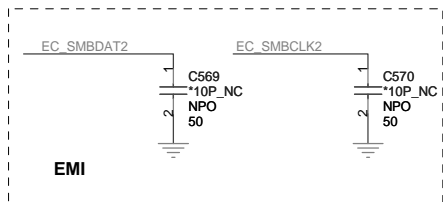
 Quanta Computer Inc.		
Project Name: GM7B		
<small>Title</small> CoversPage		
<small>Size</small>	<small>Document Number</small> GM7B_MB	<small>Rev</small> F3A
<small>Date: Monday, September 13, 2010</small> <small>Sheet 1 of 54</small>		

System Block Diagram of GM7B





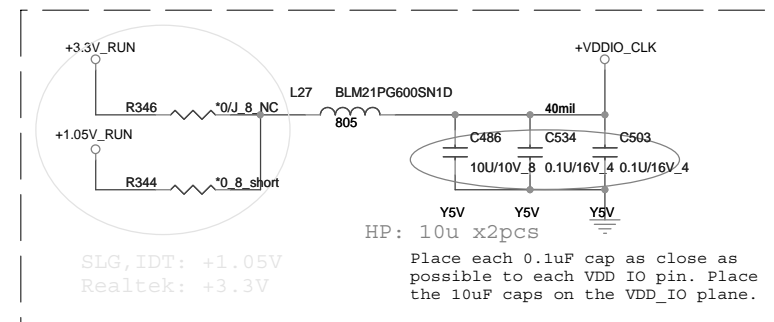
Add capacitor pads for improving WWAN.



PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V, Max 3.465V.

Quanta Computer Inc.
Project Name: **GM7B**

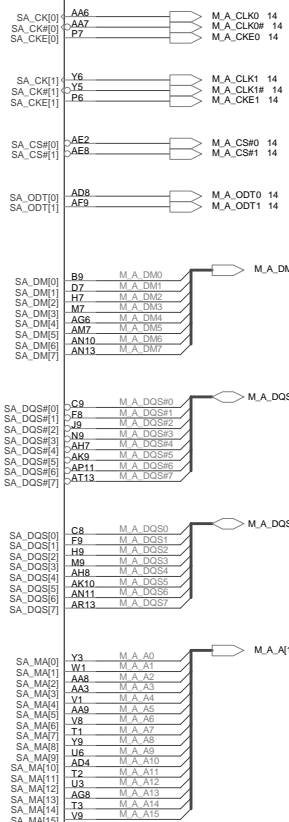
Title: CoverPage		
Size: GM7B_MB	Document Number: GM7B_MB	Rev: F3A
Date: Monday, September 13, 2010		
Sheet 3 of 54		

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U33C

14,15 M_A_DQ[8:0] M_A_DQ0 A10 M_A_DQ1 C10 M_A_DQ2 C7 M_A_DQ3 A7 M_A_DQ4 B10 M_A_DQ5 D10 M_A_DQ6 E10 M_A_DQ7 A8 M_A_DQ8 D8 M_A_DQ9 F10 M_A_DQ10 E6 M_A_DQ11 F7 M_A_DQ12 E9 M_A_DQ13 B7 M_A_DQ14 E7 M_A_DQ15 C6 M_A_DQ16 H10 M_A_DQ17 G8 M_A_DQ18 K7 M_A_DQ19 J8 M_A_DQ20 G7 M_A_DQ21 G10 M_A_DQ22 J7 M_A_DQ23 J7 M_A_DQ24 L7 M_A_DQ25 M6 M_A_DQ26 L6 M_A_DQ27 L5 M_A_DQ28 L6 M_A_DQ29 K8 M_A_DQ30 N8 M_A_DQ31 P9 M_A_DQ32 A5 M_A_DQ33 A5 M_A_DQ34 AK6 M_A_DQ35 AK7 M_A_DQ36 A6 M_A_DQ37 AG5 M_A_DQ38 AJ7 M_A_DQ39 AJ6 M_A_DQ40 AJ10 M_A_DQ41 AJ9 M_A_DQ42 AL10 M_A_DQ43 AK12 M_A_DQ44 AK8 M_A_DQ45 AL7 M_A_DQ46 AK11 M_A_DQ47 AL8 M_A_DQ48 AN8 M_A_DQ49 AM10 M_A_DQ50 AR11 M_A_DQ51 AL11 M_A_DQ52 AM9 M_A_DQ53 AN9 M_A_DQ54 AT11 M_A_DQ55 AP12 M_A_DQ56 AM12 M_A_DQ57 AN12 M_A_DQ58 AM13 M_A_DQ59 AT14 M_A_DQ60 AT12 M_A_DQ61 AL13 M_A_DQ62 AR14 M_A_DQ63 AP14

DDR SYSTEM MEMORY A

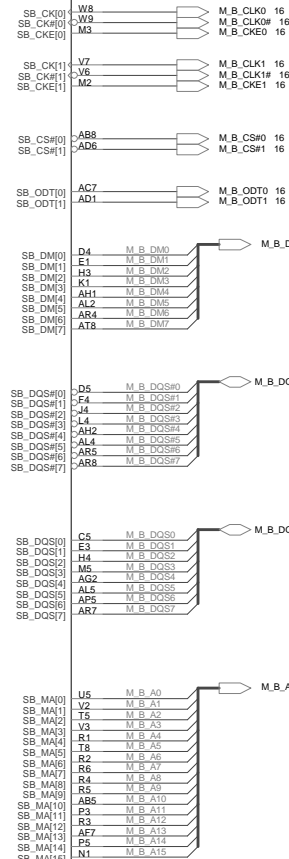


P298927-3641-01F

U33D

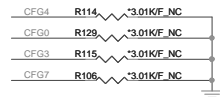
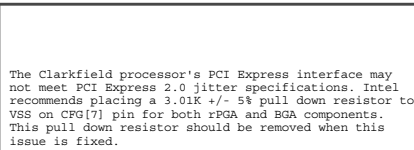
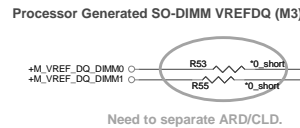
M_B_DQ0 B5 M_B_DQ1 A5 M_B_DQ2 C3 M_B_DQ3 B3 M_B_DQ4 E4 M_B_DQ5 A6 M_B_DQ6 A4 M_B_DQ7 C4 M_B_DQ8 D1 M_B_DQ9 D2 M_B_DQ10 C2 M_B_DQ11 F1 M_B_DQ12 C2 M_B_DQ13 F5 M_B_DQ14 F3 M_B_DQ15 G4 M_B_DQ16 H6 M_B_DQ17 G2 M_B_DQ18 J6 M_B_DQ19 J3 M_B_DQ20 G1 M_B_DQ21 G5 M_B_DQ22 J1 M_B_DQ23 J5 M_B_DQ24 J5 M_B_DQ25 L3 M_B_DQ26 L3 M_B_DQ27 M1 M_B_DQ28 K4 M_B_DQ29 K4 M_B_DQ30 M4 M_B_DQ31 N5 M_B_DQ32 AE3 M_B_DQ33 AG1 M_B_DQ34 AJ3 M_B_DQ35 AK1 M_B_DQ36 AG4 M_B_DQ37 AG3 M_B_DQ38 AJ4 M_B_DQ39 AH4 M_B_DQ40 AK3 M_B_DQ41 AK4 M_B_DQ42 AM6 M_B_DQ43 AN2 M_B_DQ44 AK5 M_B_DQ45 AK2 M_B_DQ46 AM4 M_B_DQ47 AM3 M_B_DQ48 AP3 M_B_DQ49 AN6 M_B_DQ50 AN6 M_B_DQ51 AN6 M_B_DQ52 AN4 M_B_DQ53 AN3 M_B_DQ54 AT2 M_B_DQ55 AT6 M_B_DQ56 AN7 M_B_DQ57 AP6 M_B_DQ58 AP9 M_B_DQ59 AT9 M_B_DQ60 AT7 M_B_DQ61 AP9 M_B_DQ62 AR10 M_B_DQ63 AT10

DDR SYSTEM MEMORY - B



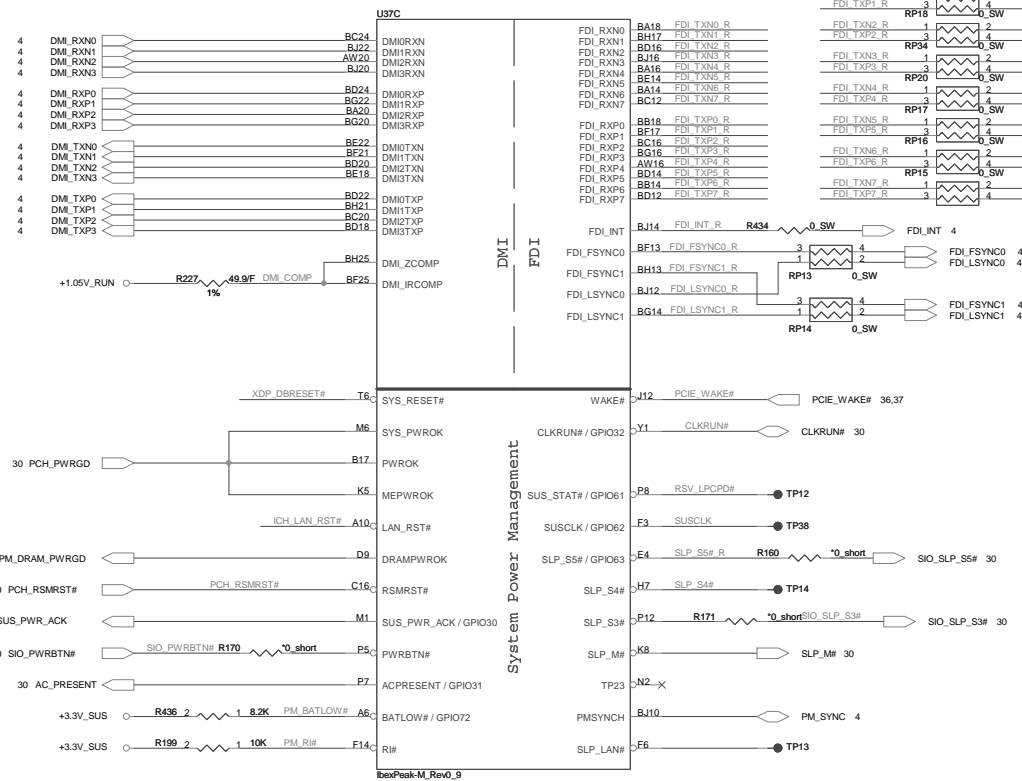
P298927-3641-01F

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

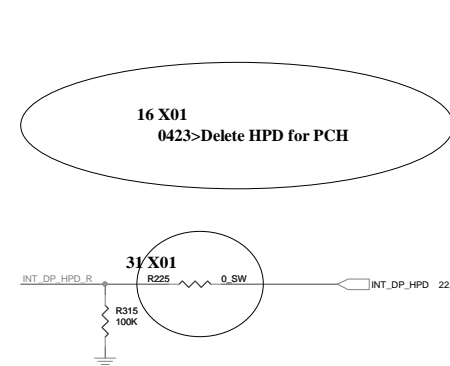
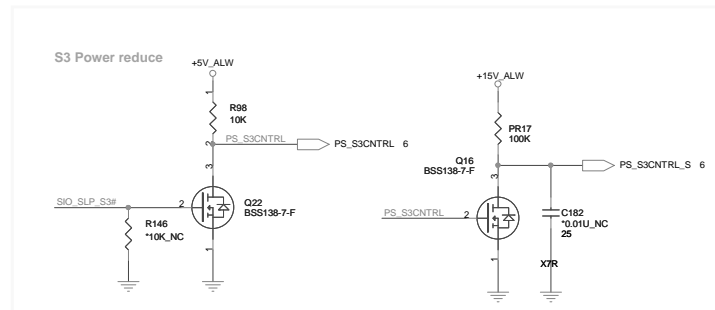
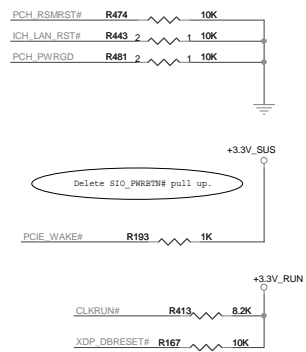
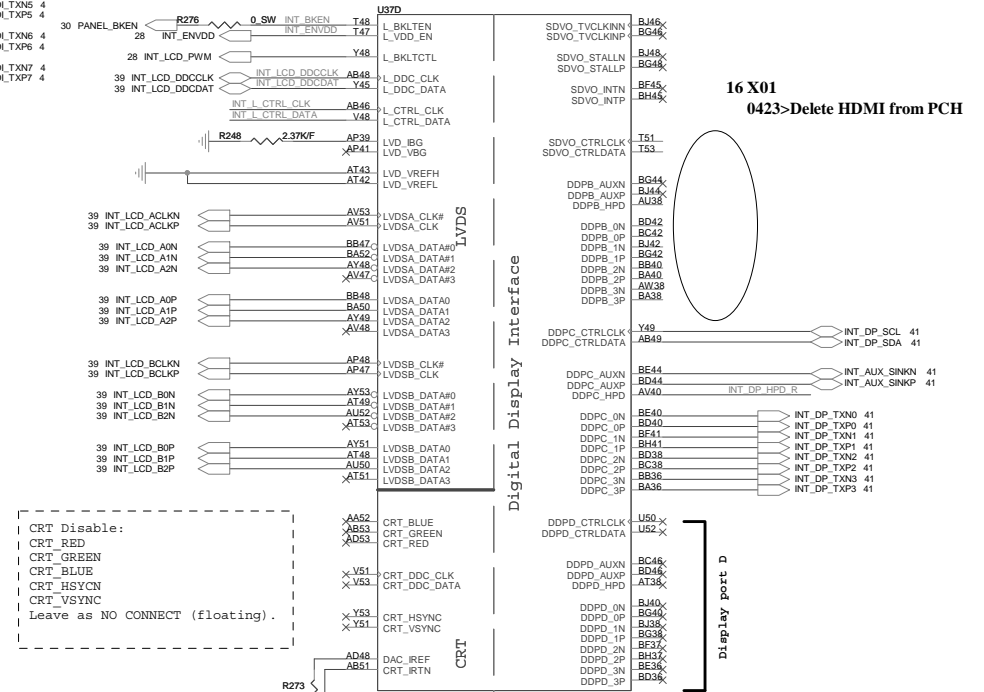


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 Clarksville (only for early samples pre-ES)	Common motherboard design	For early samples pre-ES1 CFD

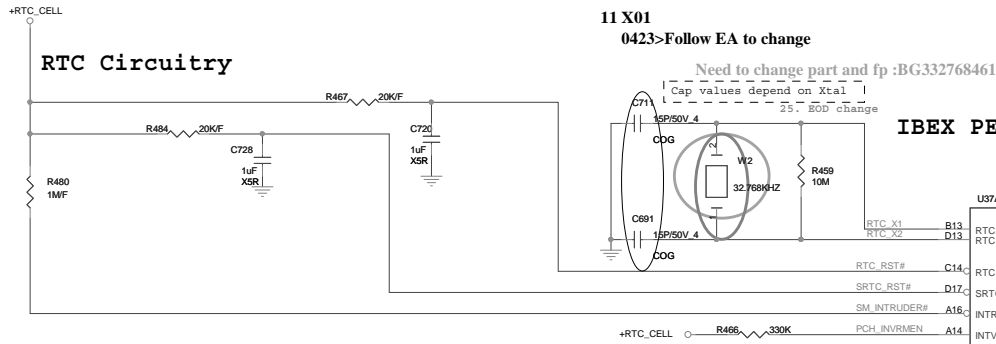
IBEX PEAK-M (DMI, FDI, GPIO)



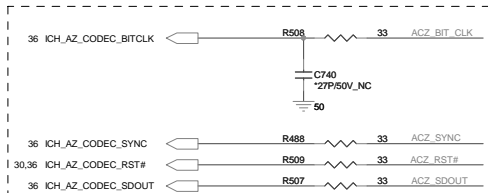
IBEX PEAK-M (LVDS, DDI)



RTC Circuitry



IBEX PEAK-M (HDA, JTAG, SATA)



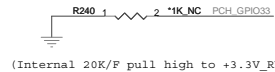
INTVRMEN - Integrated SUS 1.1V VRN Enable
High - Enable Internal VRs

0 ohm resistor within 0.5 inch of pin

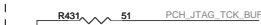
Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

Flash Descriptor Security Override

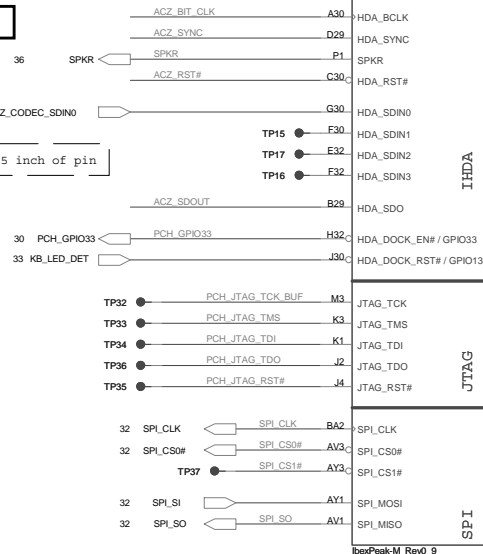
GPI033
Low = Enabled
High = Disabled



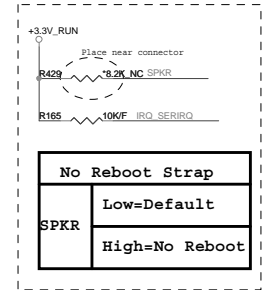
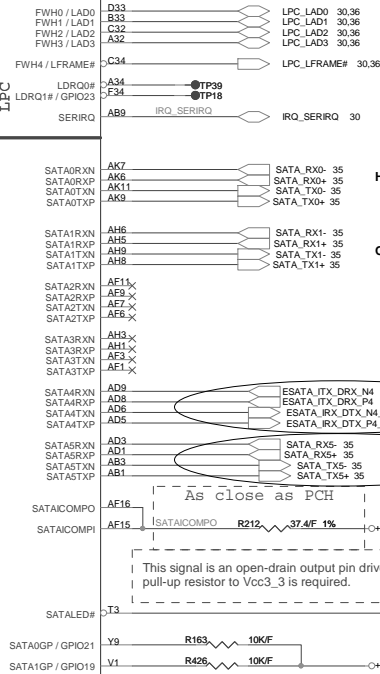
Note : GPI033 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



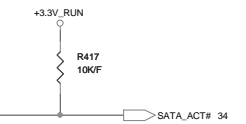
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.



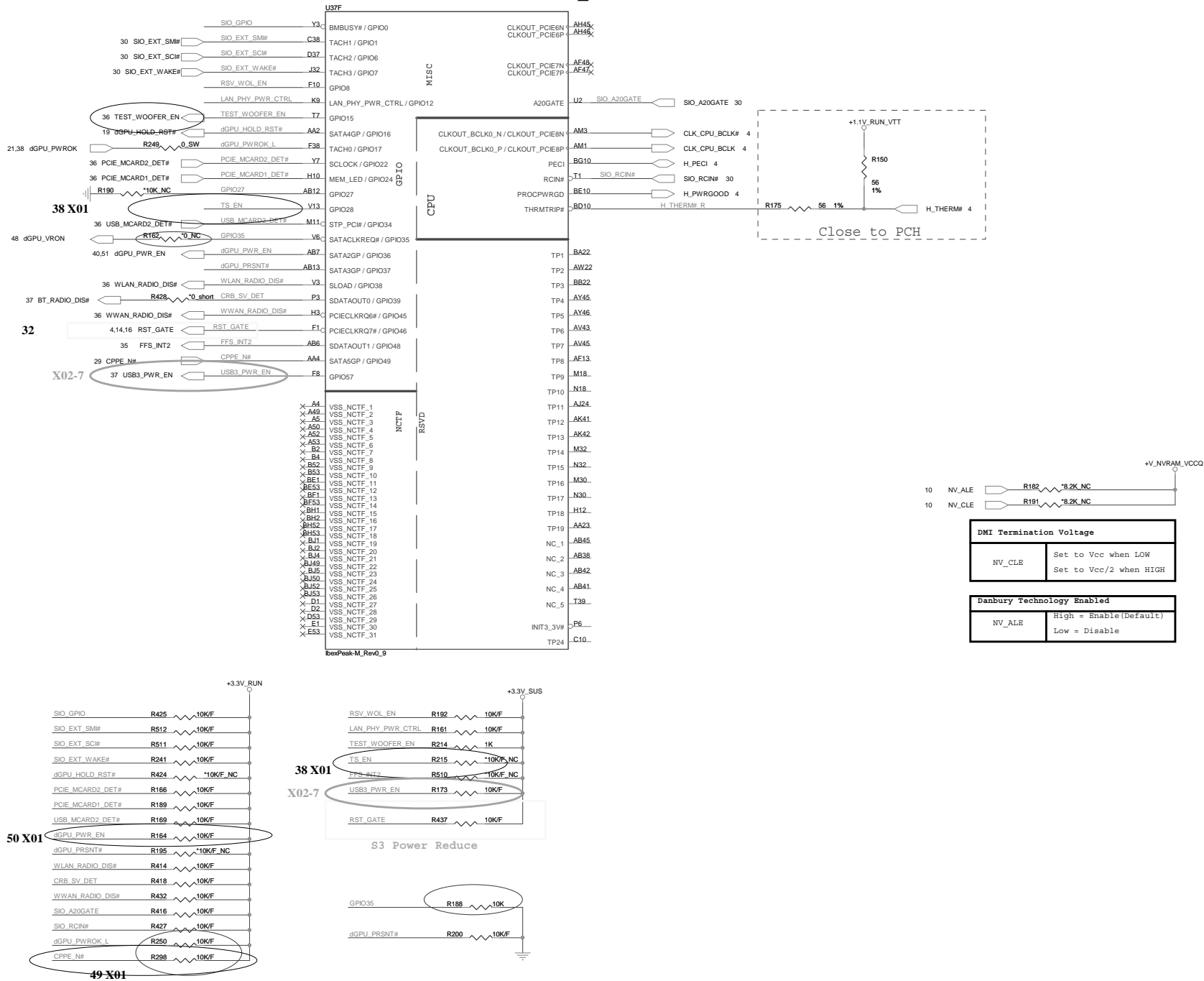
IBEX Peak-M_Rev0.9



5 X01
0410>Reverse eSATA TX/RX
7 X01
0413>Reverse SATA5 TX+/-



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



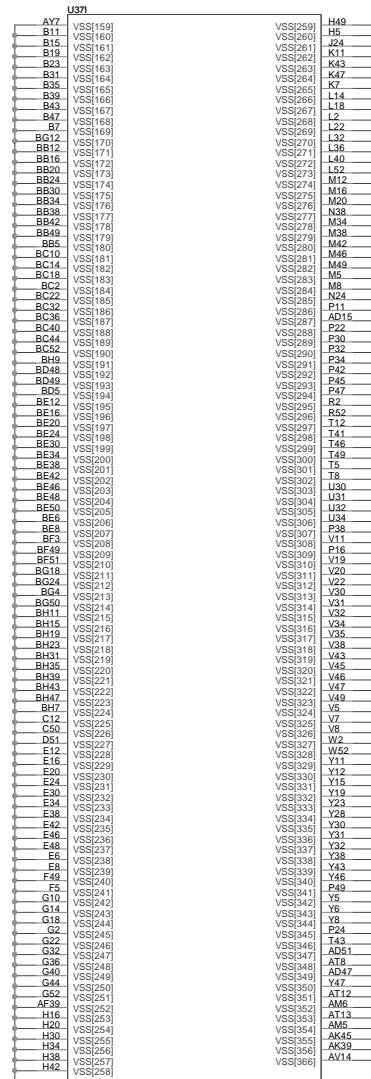
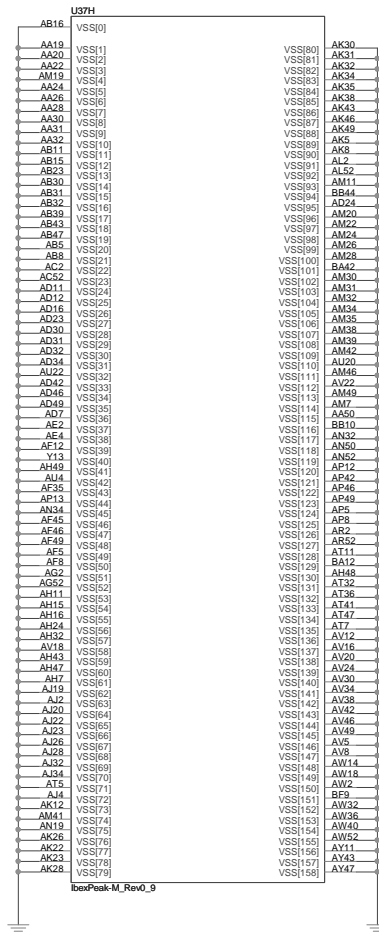
+V_NVRAM_VCCO	
10 NV_ALE	R182 *8.2K NC
10 NV_CLE	R191 *8.2K NC
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH
Danbury Technology Enabled	
NV_ALE	High = Enable(Default) Low = Disable

POWER

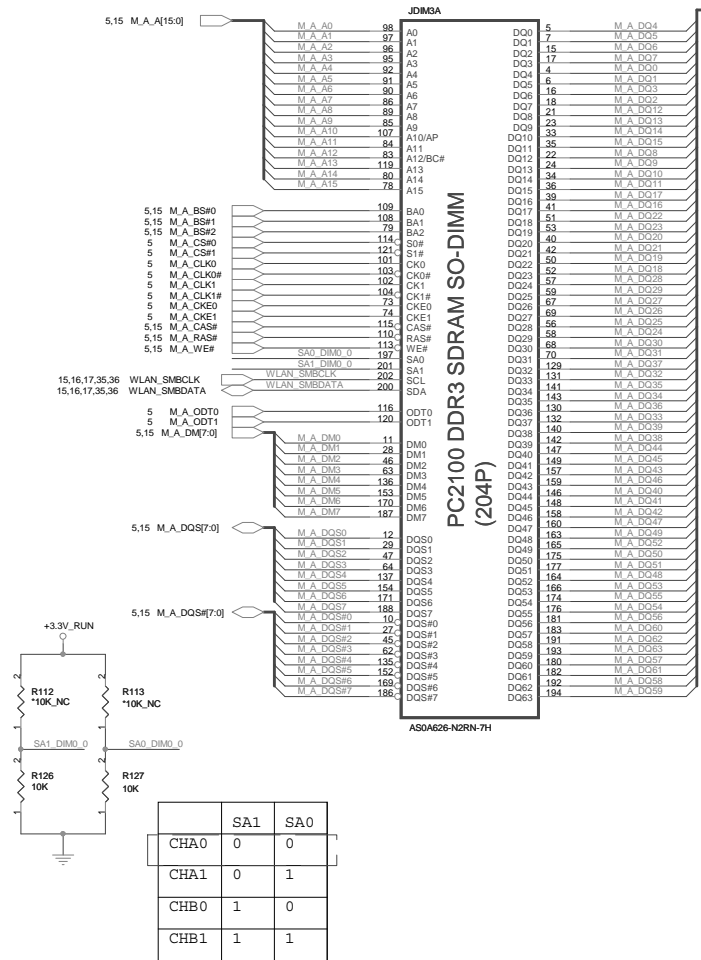


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PCH 5/6 (POWER)			
Size	Document Number		Rev
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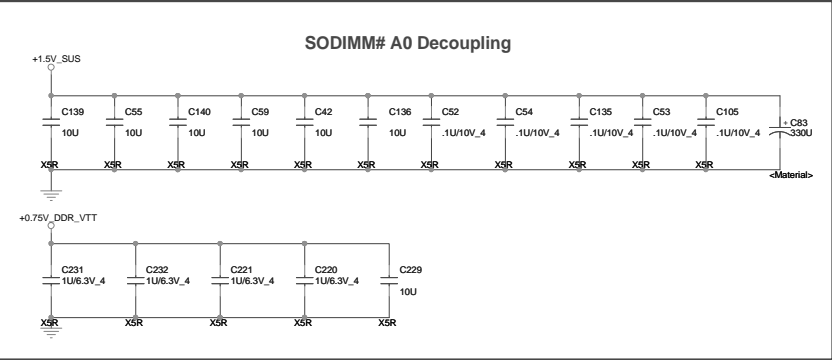
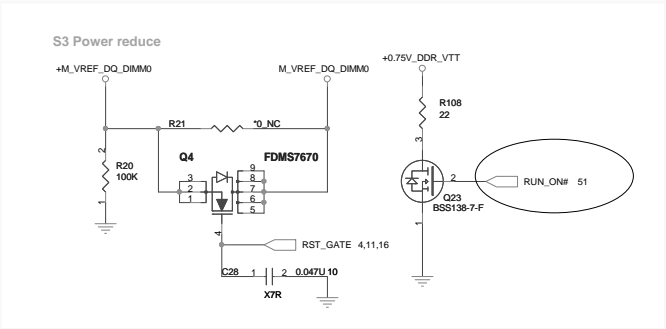
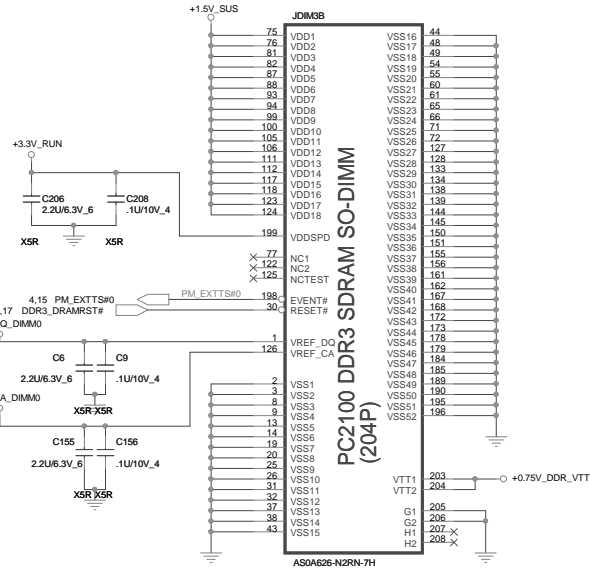
IBEX PEAK-M (GND)



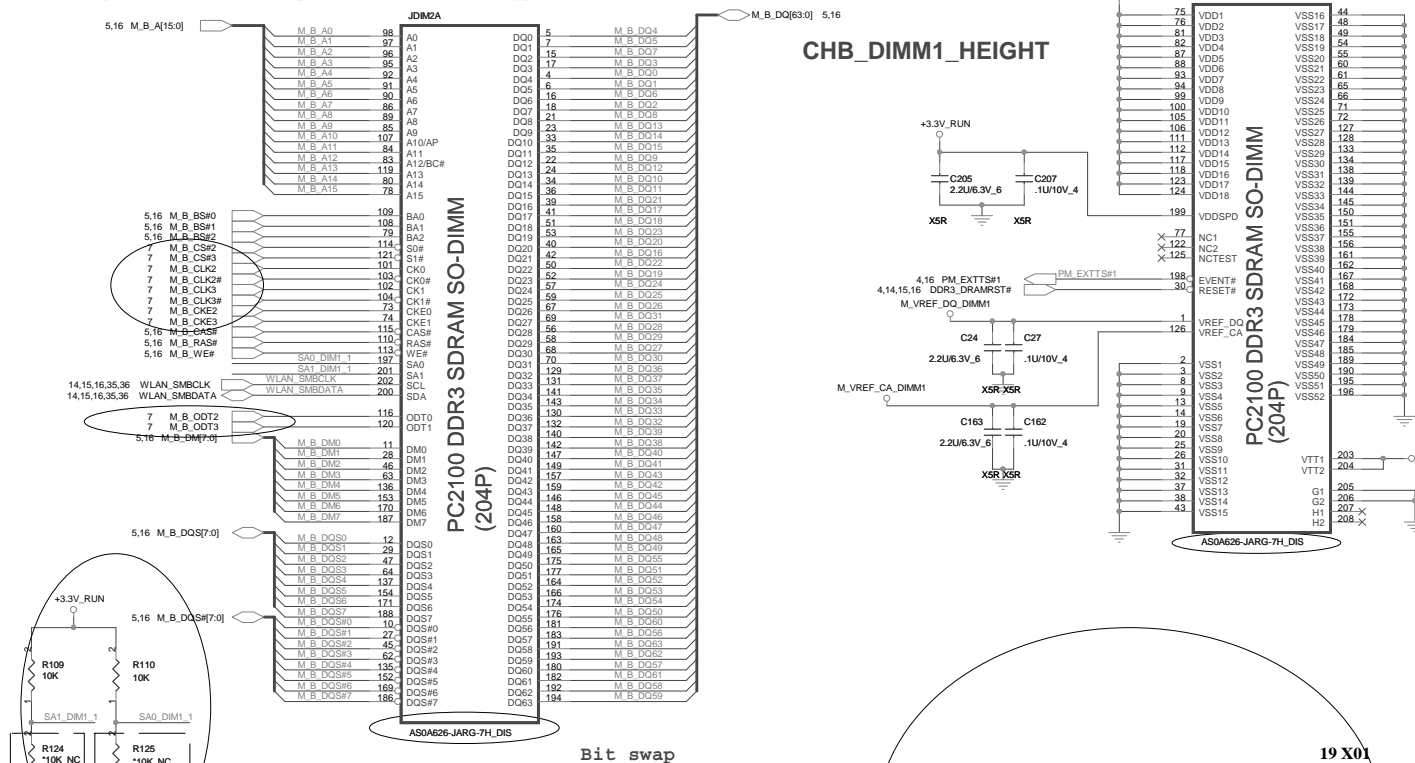
1123GC: Update JDIM7002 footprint 5.2mm, Ruv type.



CHA_DIMM0_HEIGHT

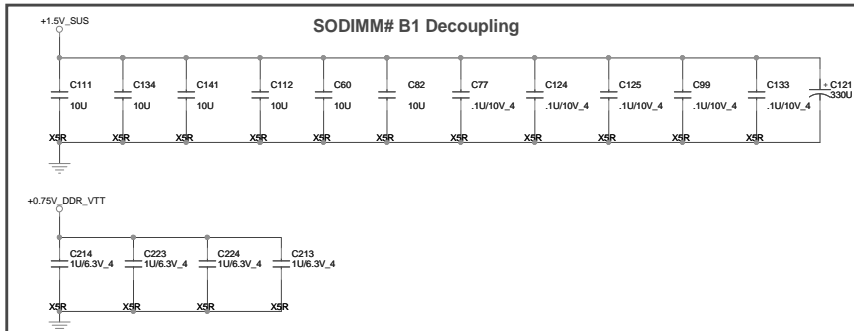


1123GC: Update JDIM7001 footprint to 9.2mm, RVS type.

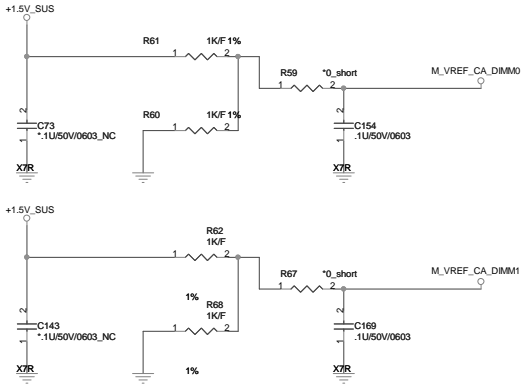
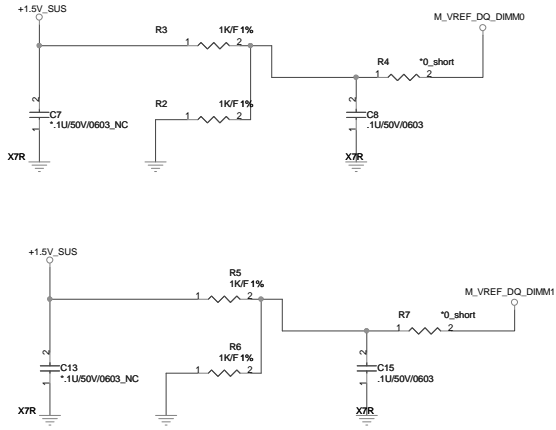


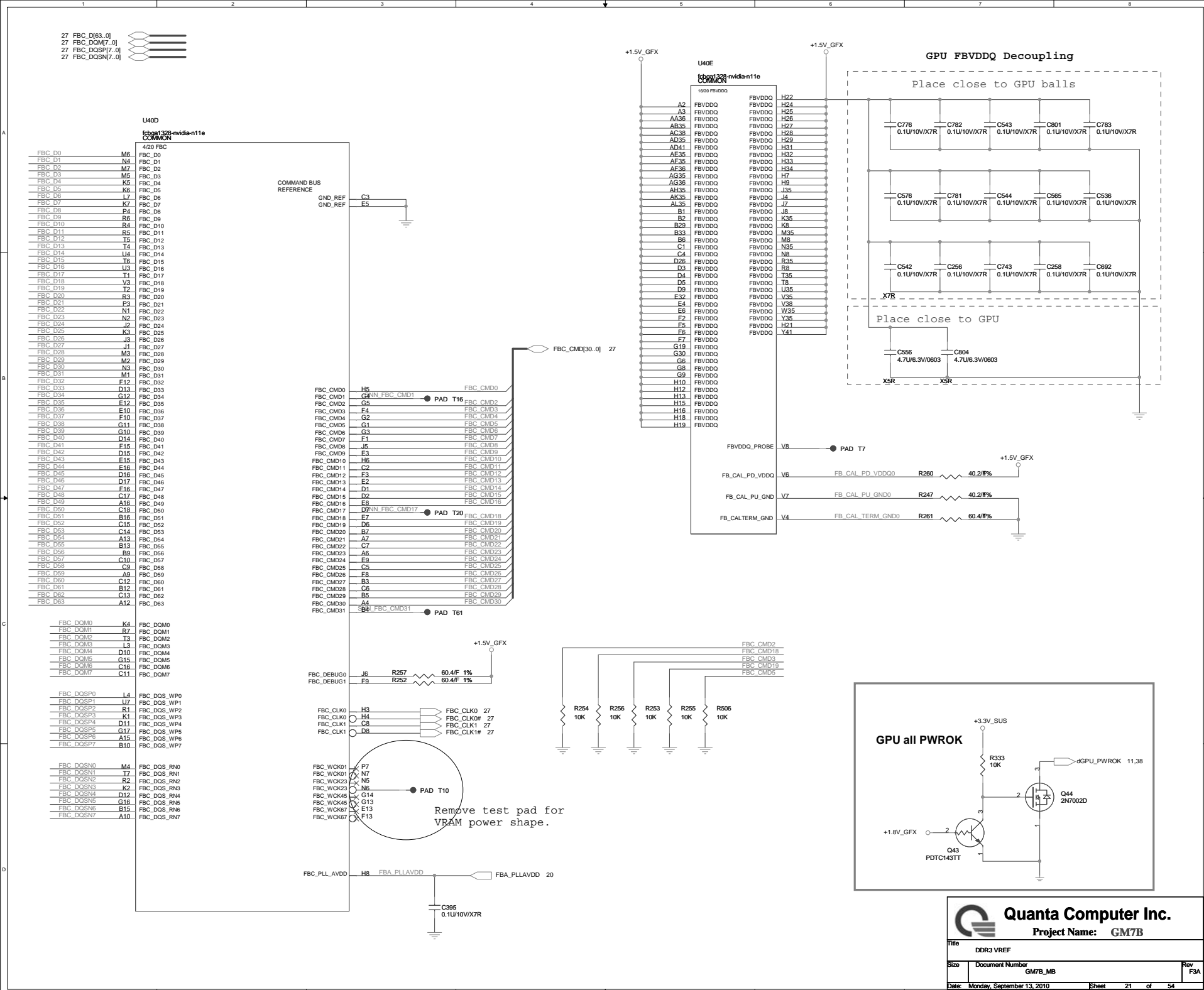
8 X01
0413>Add_DIS for SODIMM

Note:
SO-DIMMA SPD Address is 0xA6
SO-DIMMA TS Address is 0x36

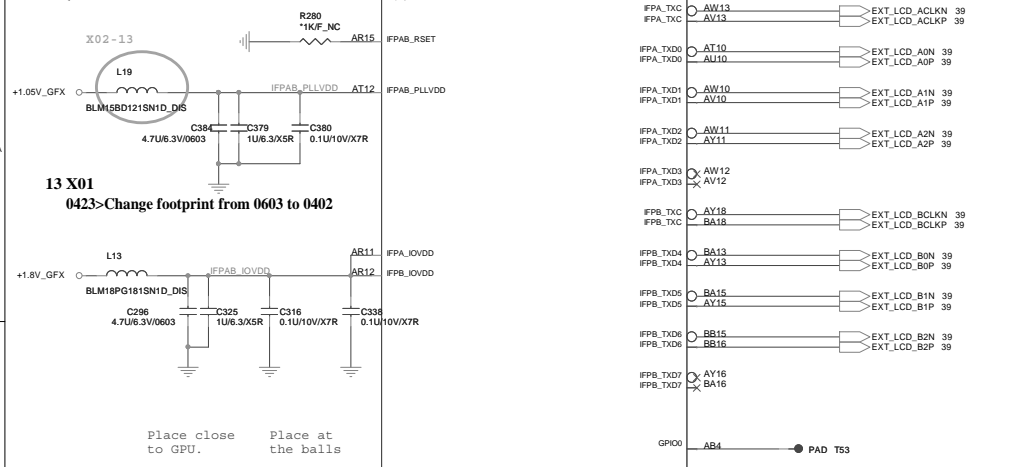


Fixed SO-DIMM VREF_DQ (M1): Default

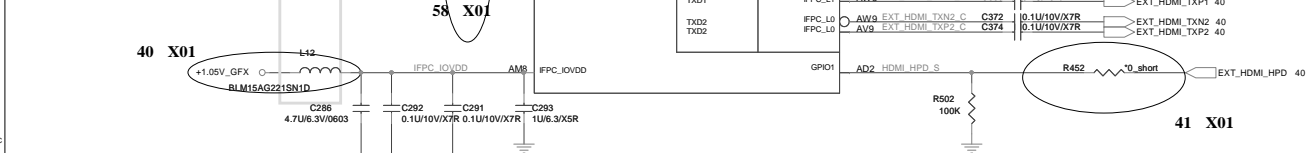




13 X01 
0423>Change footprint from 0603 to 0402



For Optimus 1.1
L9,L12,R296 pop

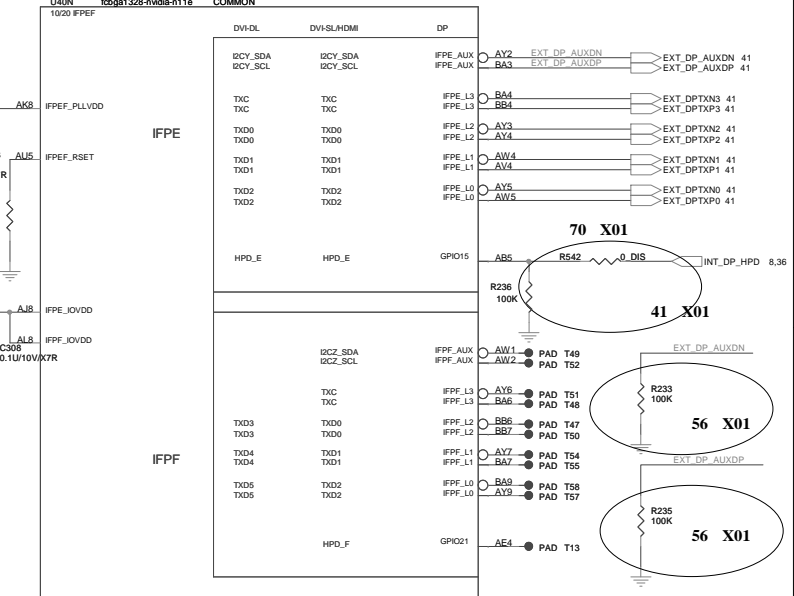
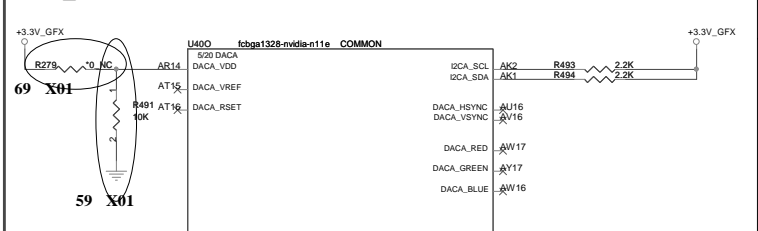


26 X01

R353 10K

20 X01

	1980	1985	1990	1995	2000	2005	2010	2015	2020
Population	76.0	80.0	84.0	88.0	92.0	96.0	100.0	104.0	108.0
GDP	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0
Government expenditure	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0
Private consumption	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0
Investment	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0
Savings	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0
Exports	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0
Imports	100.0	110.0	120.0	130.0	140.0	150.0	160.0	170.0	180.0

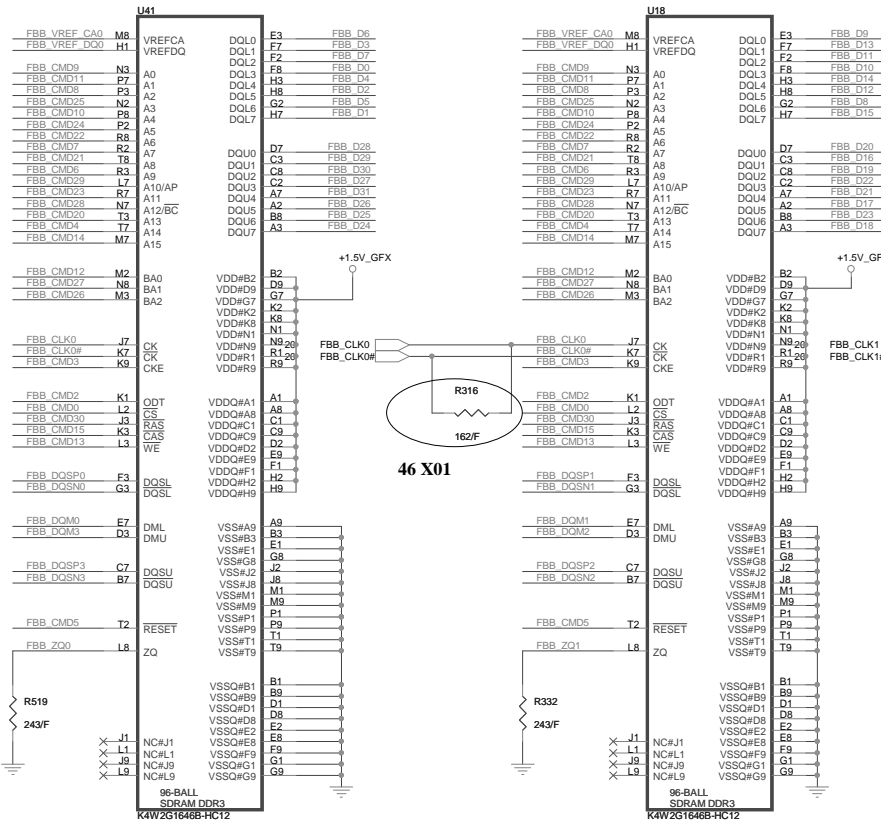
69 ~~X01~~

Quanta Computer Inc.
Project Name: GM7B

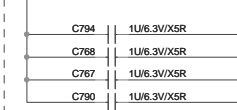
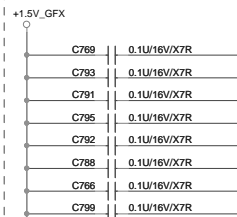
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Size	Document Number						Rev
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20 FBB_CMD[30..0]
20 FBB_DQ[63..0]
20 FBB_DQM[7..0]
20 FBB_DQSP[7..0]
20 FBB_DQSN[7..0]

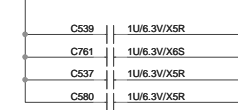
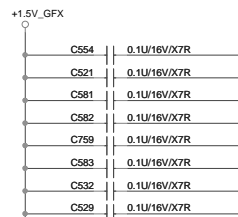
Memory Lower Partition B



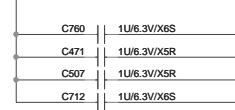
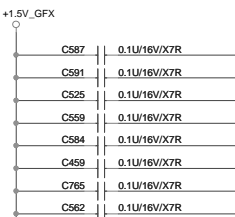
Decoupling for U1



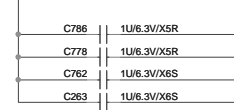
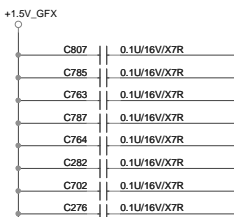
Decoupling for U2



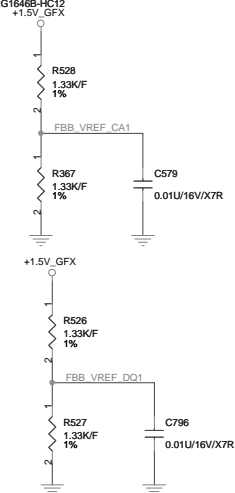
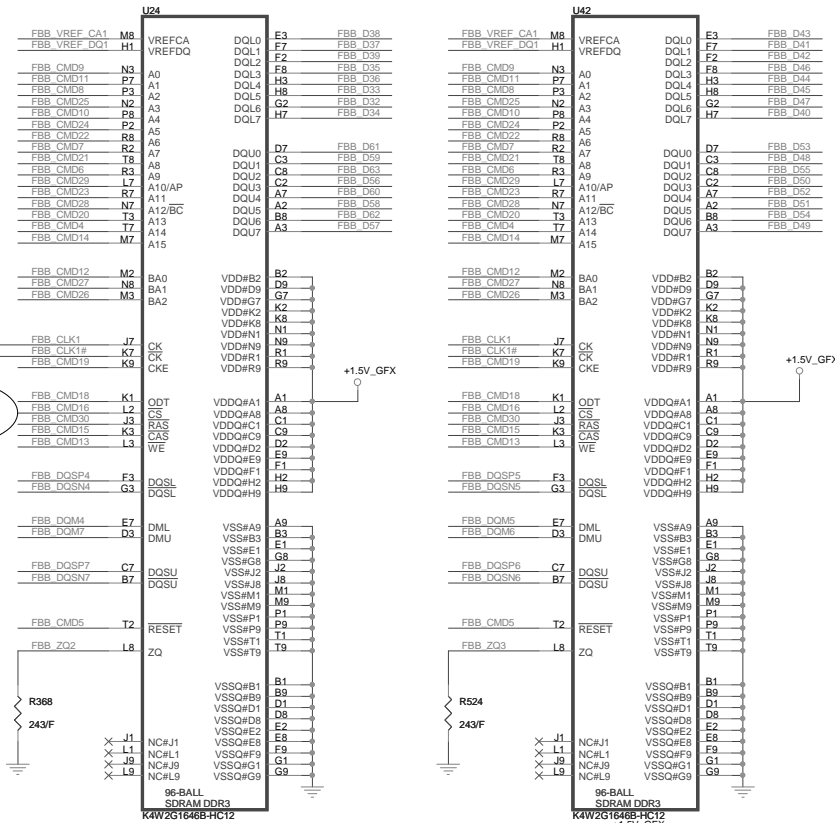
Decoupling for U3



Decoupling for U4



Memory Upper Partition B



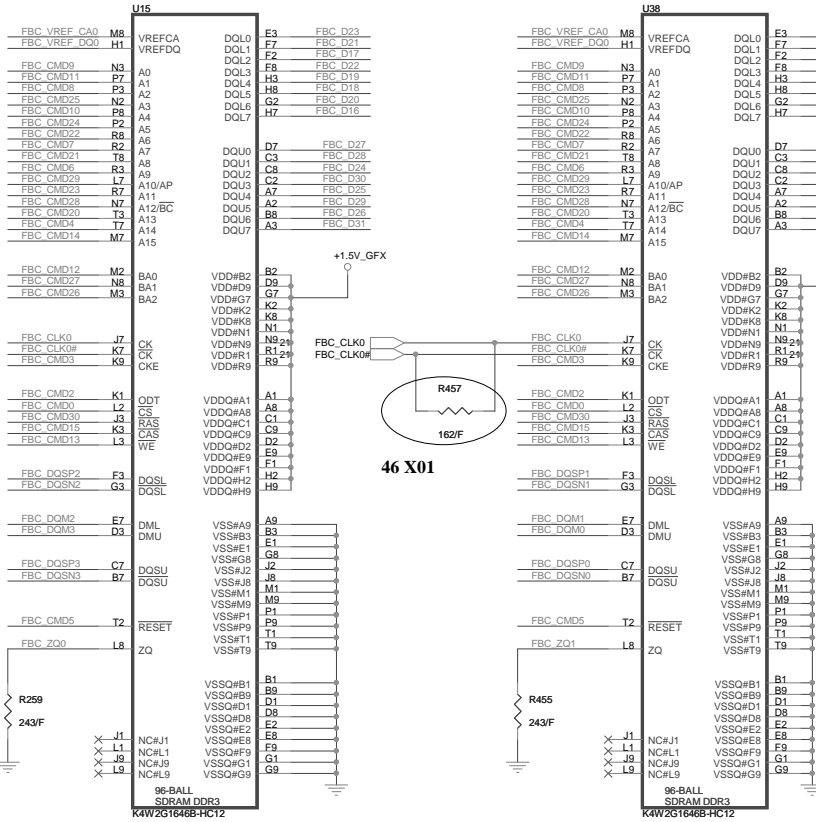
Quanta Computer Inc.

Project Name: GM7B

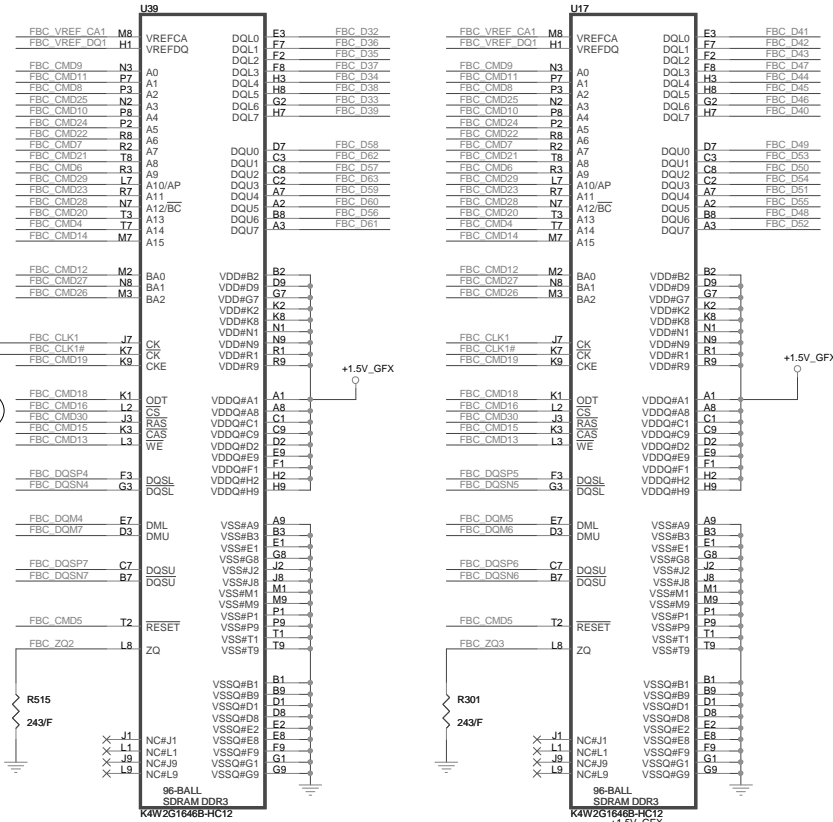
Title	DDR3 VREF		
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21 FBC_CMD30[30..0]
21 FBC_DQ[63..0]
21 FBC_DQM[7..0]
21 FBC_DQSP[7..0]
21 FBC_DQSN[7..0]

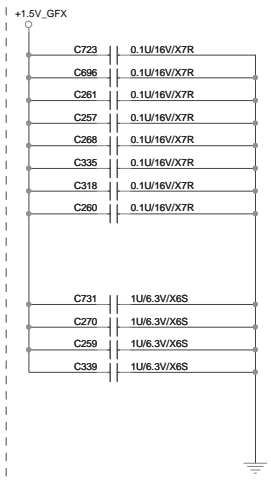
Memory Lower Partition C



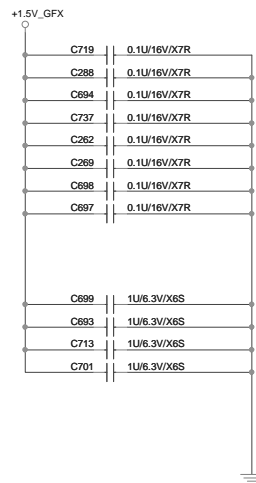
Memory Upper Partition C



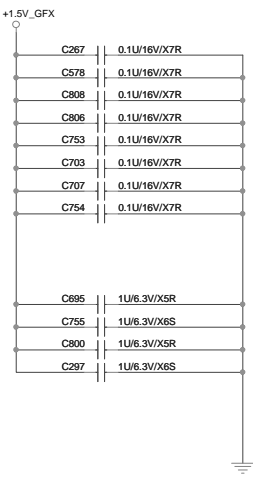
Decoupling for U1



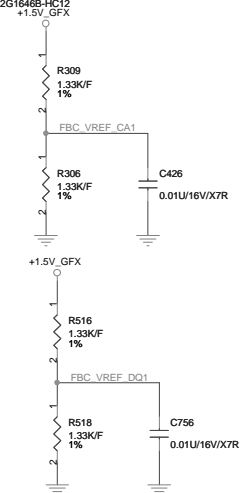
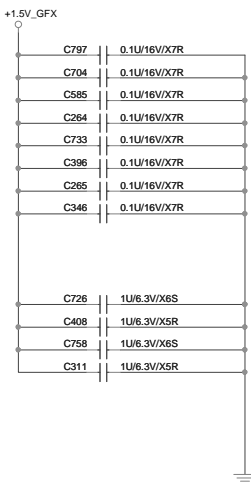
Decoupling for U2



Decoupling for U3



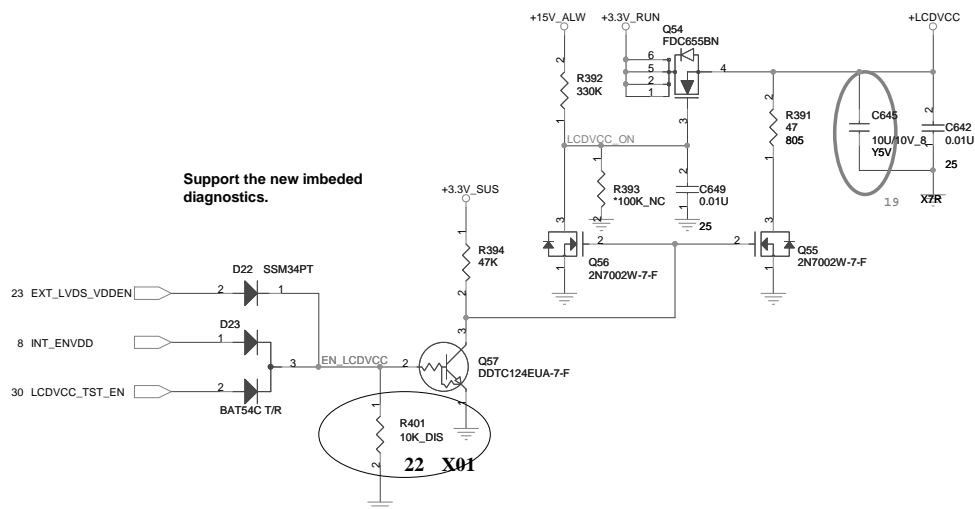
Decoupling for U4



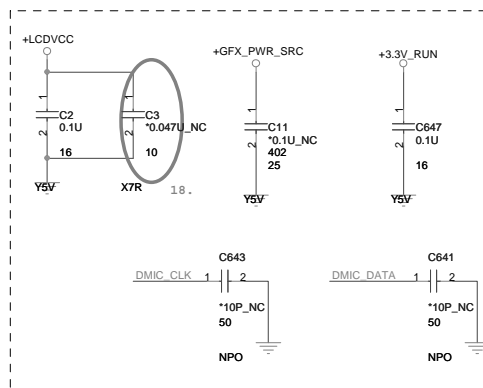
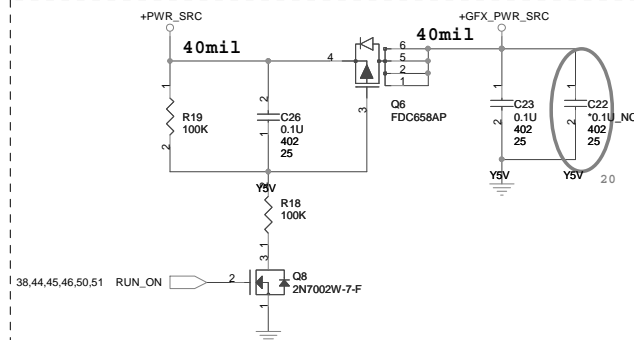
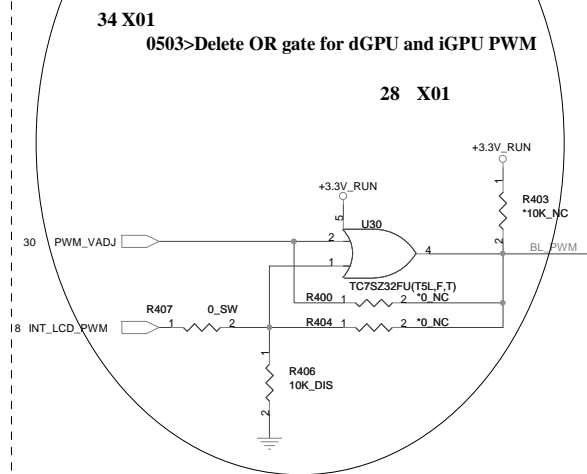
Quanta Computer Inc.
Project Name: GM7B

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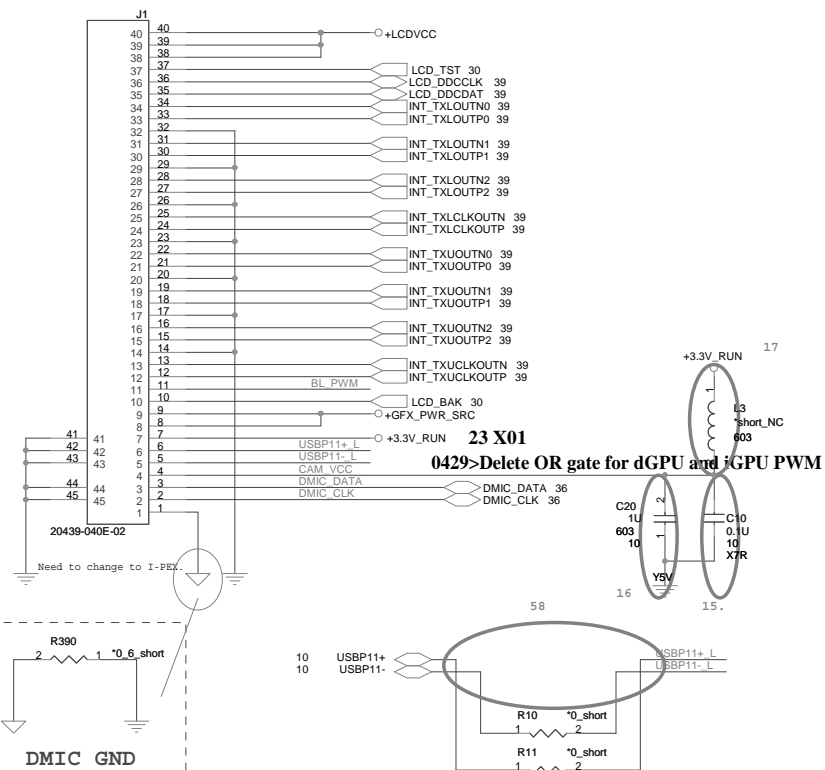
Panel VCC



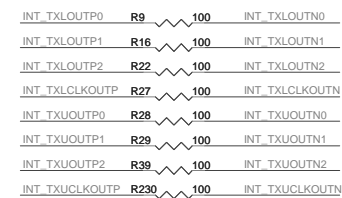
Backlight Control



40Pin LVDS & Array Microphone & Camera Connector



EMC Reserve



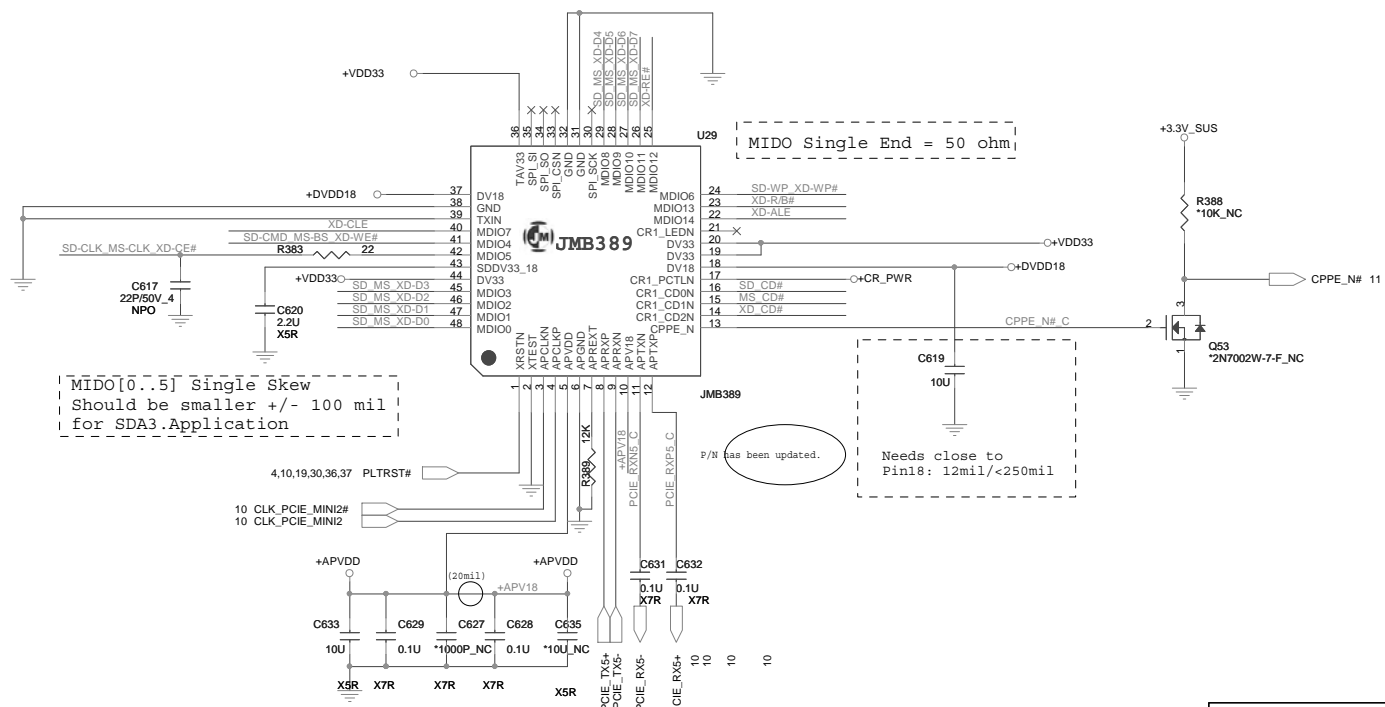
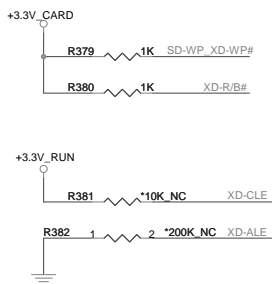
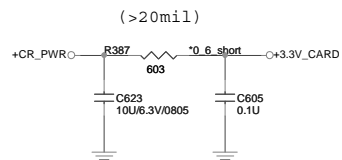
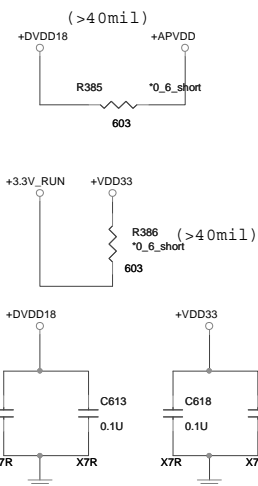
Please R close to pin of LCD connector, J1

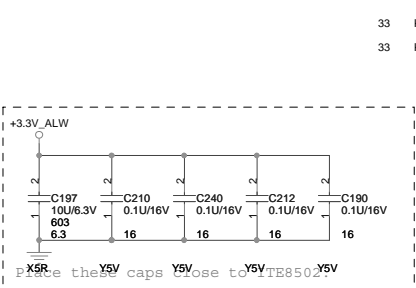
**Quanta Computer Inc.**

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Title			
CoverPage			
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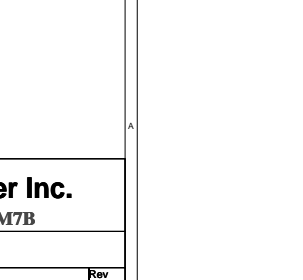
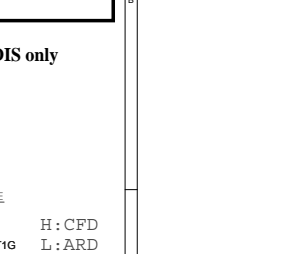
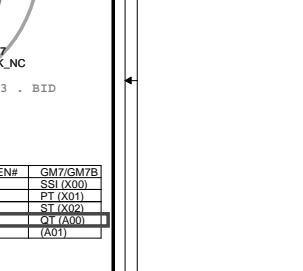
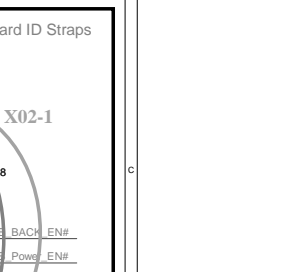
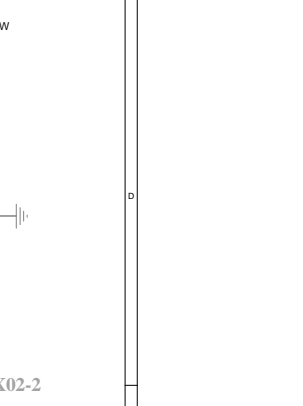
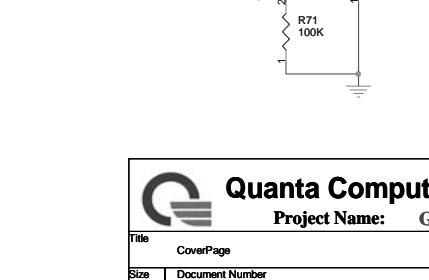
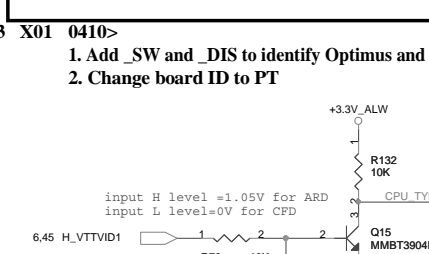
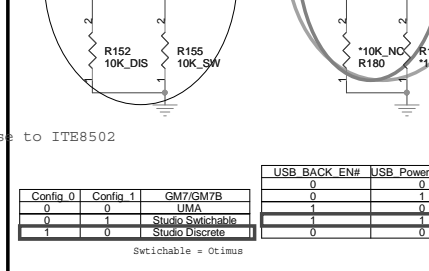
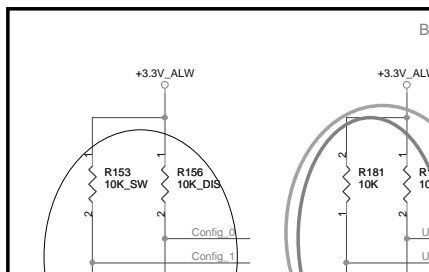
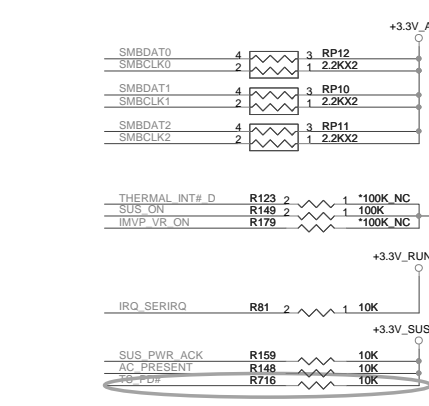
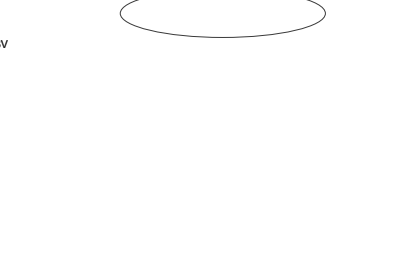
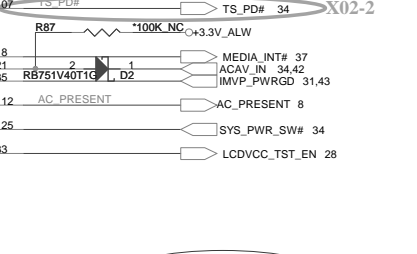
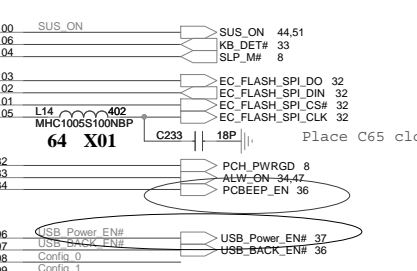
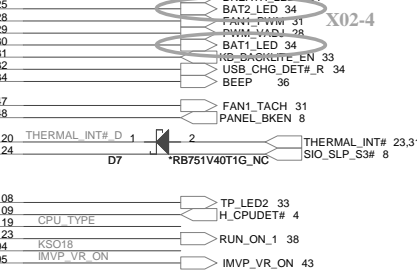
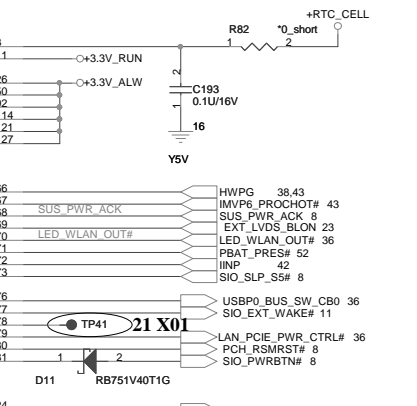
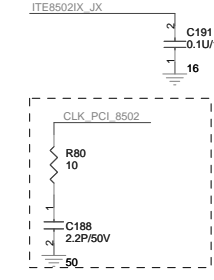
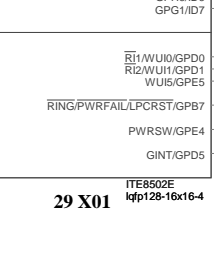
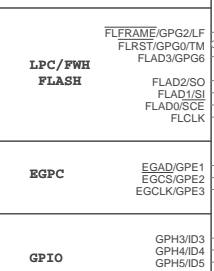
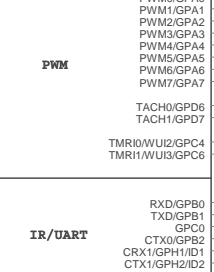
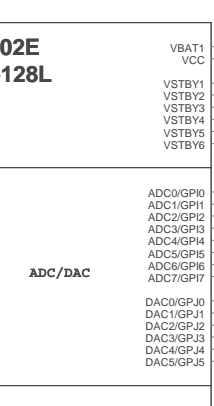
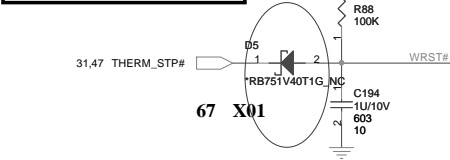
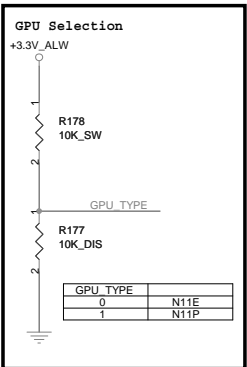
PIN	Result	MS	MS	MS	XD
MD1000	SD/MMC/MS/xd	SD D0	MS D0	MS D0	XD D0
MD1001		SD D1	MS D1	MS D1	XD D1
MD1002		SD D2	MS D2	MS D2	XD D2
MD1003		SD D3	MS D3	MS D3	XD D3
MD1004		SD CMD	MS SS	MS SS	XD WE#
MD1005		SD CLK	MS CLK	MS CLK	XD CE#
MD1006		SD WP		MS WP#	XD WP#
MD1007				MS CLE	XD CLE
MD1008		MMC D4	MS D4	MS D4	XD D4
MD1009		MMC D5	MS D5	MS D5	XD D5
MD1010		MMC D6	MS D6	MS D6	XD D6
MD1011		MMC D7	MS D7	MS D7	XD D7
MD1012					XD RE
MD1013					XD R/B#
MD1014					XD ALE
CRI_LB00		SD LEDB	MS LEDB	MS LEDB	XD LB0#
CRI_PCTLN		SD PWR#	MS PWR#	MS PWR#	XD PWR#
CRI_CD0		SD CD#		MS CD#	
CRI_CD1					
CRI_CD2					XD CD#

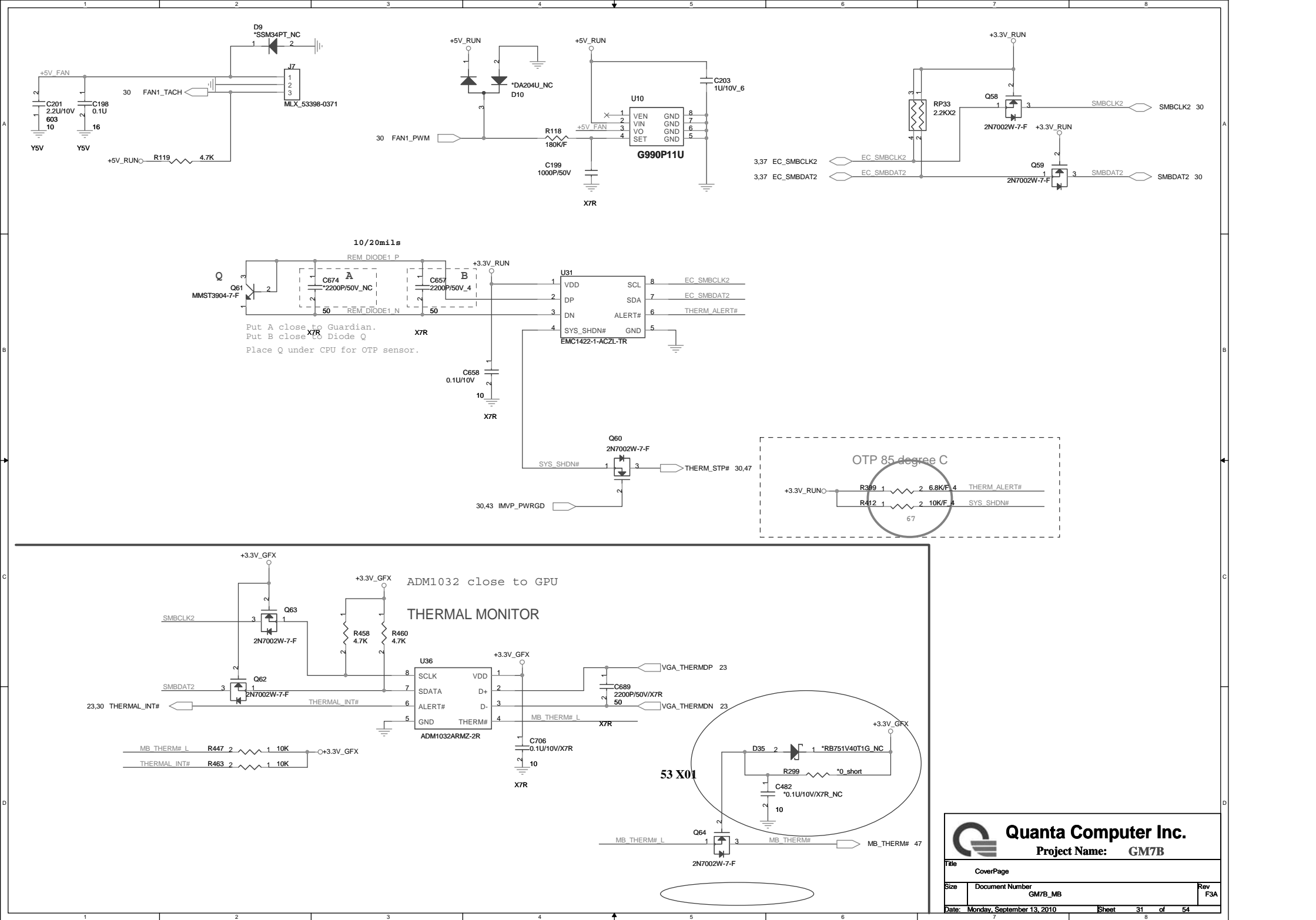




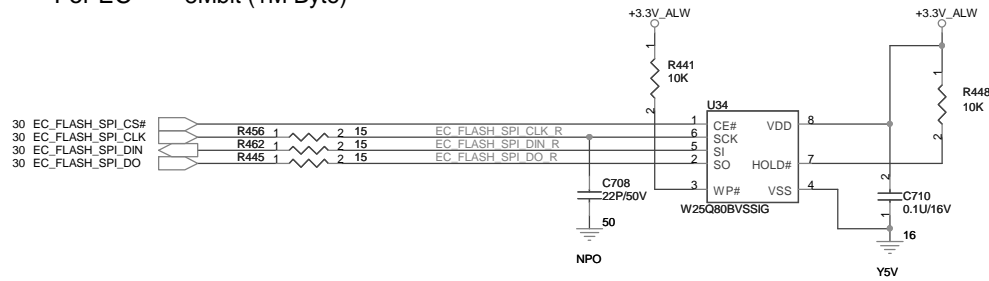
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k
pull-up to +V3.3S.

Charge and BAT
PCH
CLK, Thermal,
VGA Thermal, and MMB



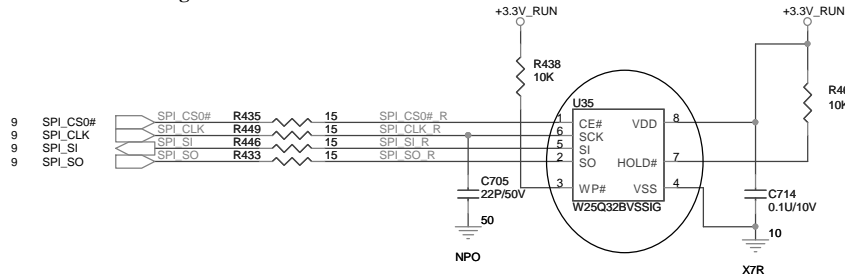


For EC 8Mbit (1M Byte)

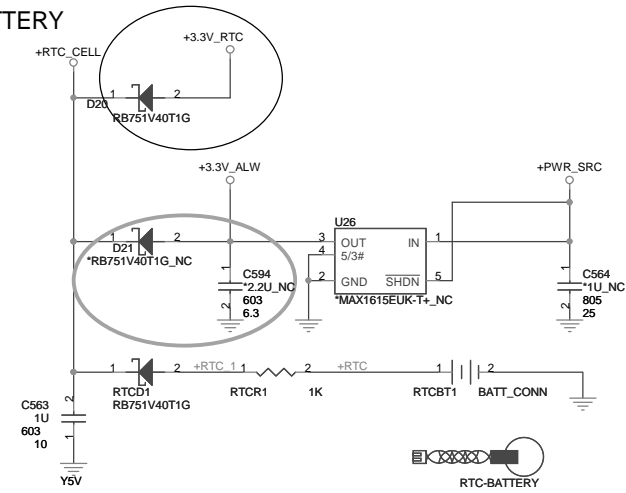


For PCH 32Mbit (4M Byte)

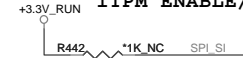
11 X01
0423>Change from 8MB to 4MB



RTC BATTERY

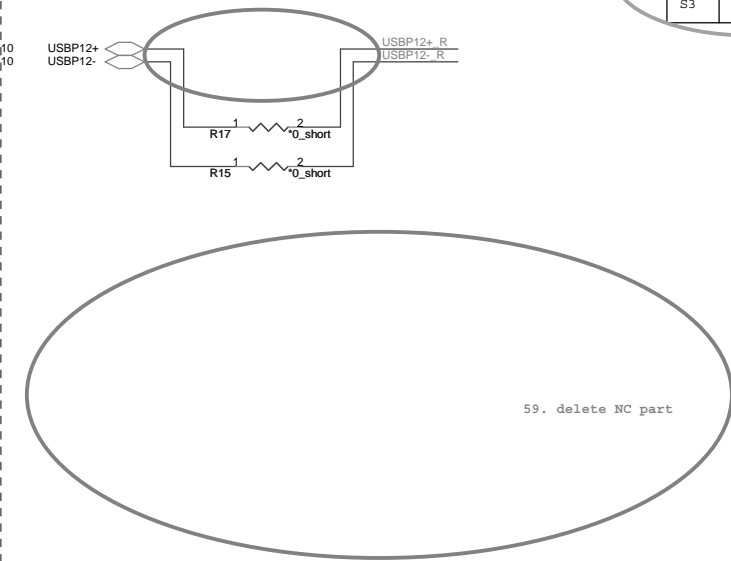
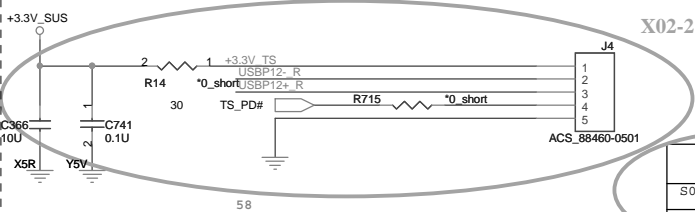


iTPM ENABLE/DISABLE

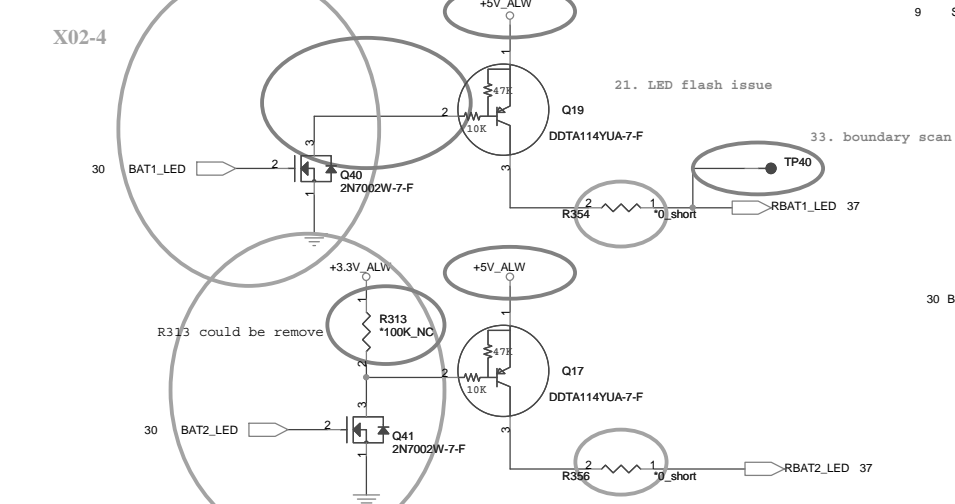


TPM Function	R712
Enable	Mount
Disable	NC (Default)

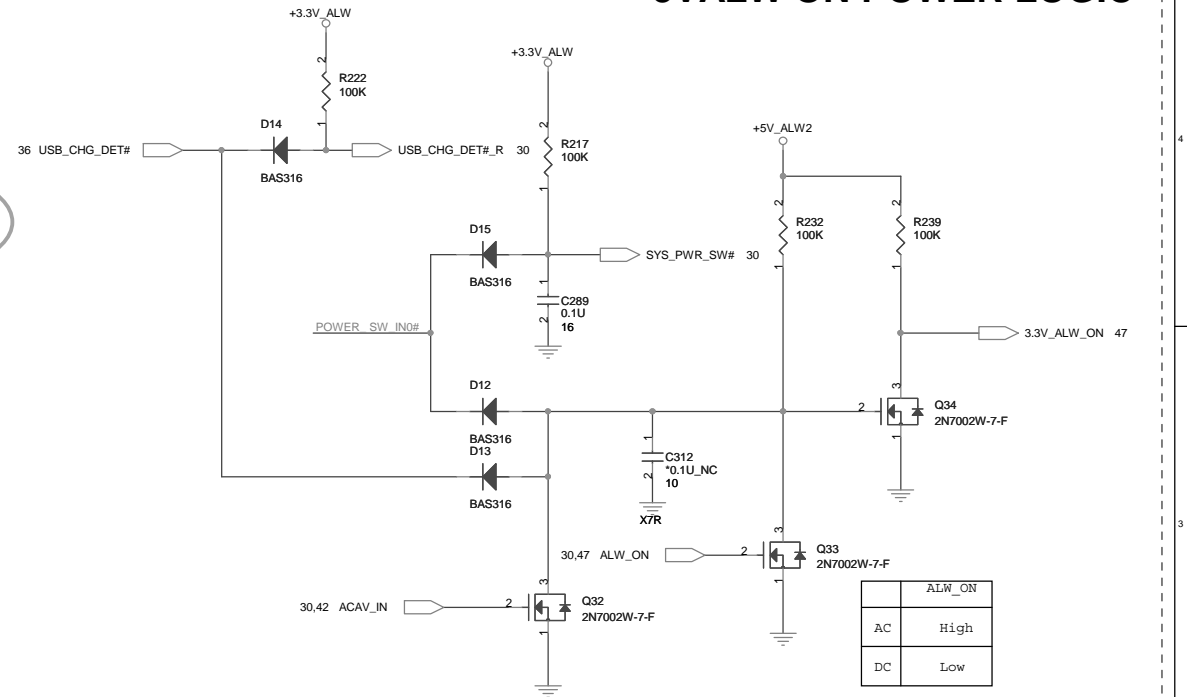
Touch Screen Module



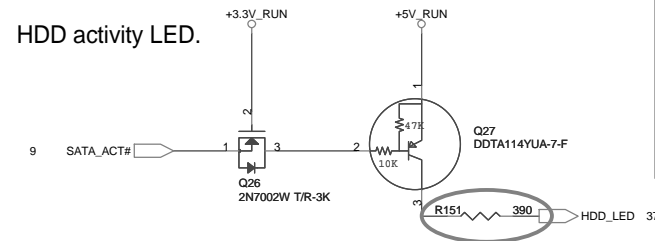
LED



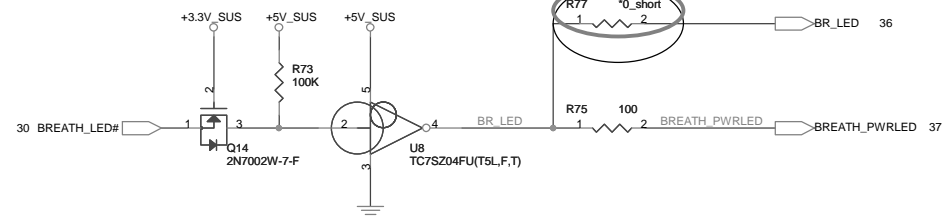
3VALW ON POWER LOGIC



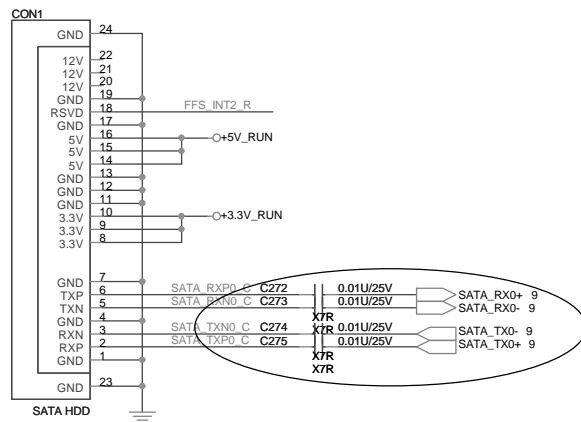
HDD activity LED.



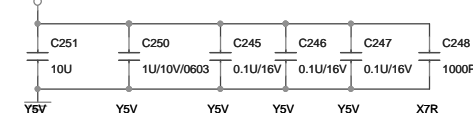
Power button for Engineer



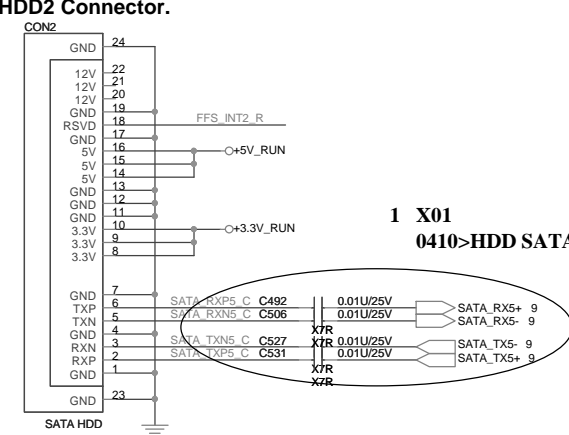
HDD0 Connector.



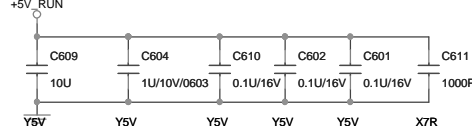
Place caps close to HDD0 connector.



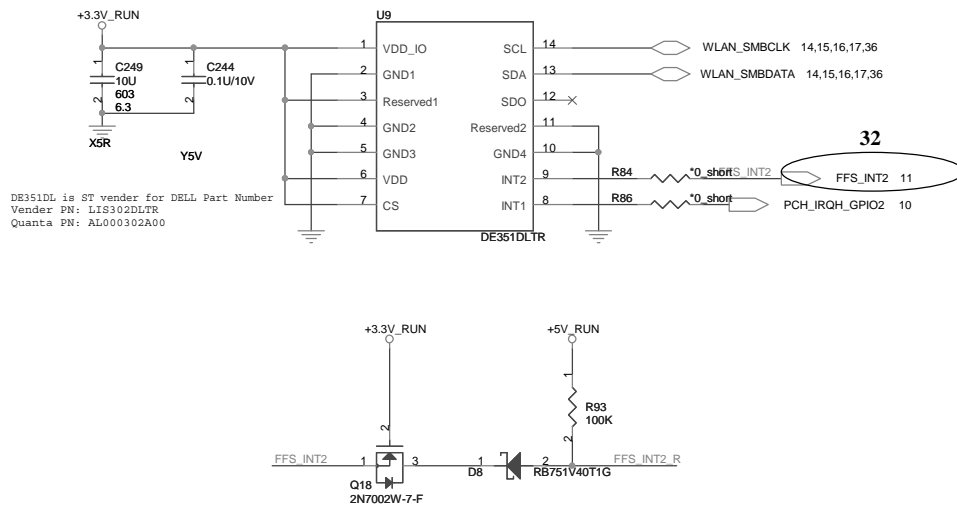
HDD2 Connector.



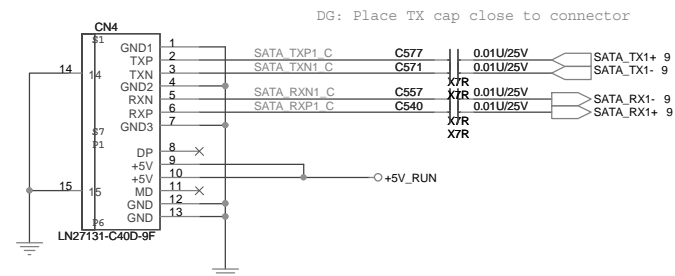
Place caps close to HDD2 connector.



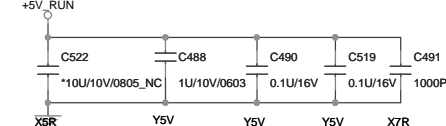
3-axis Fall Sensor (HDD data protector)



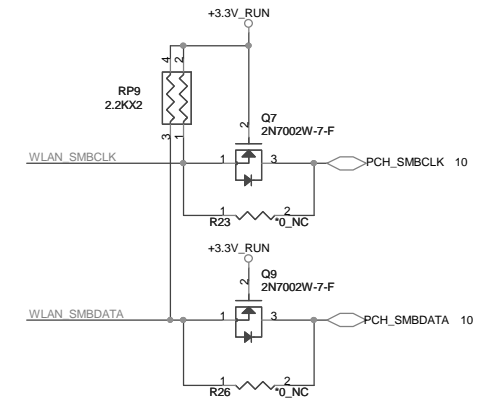
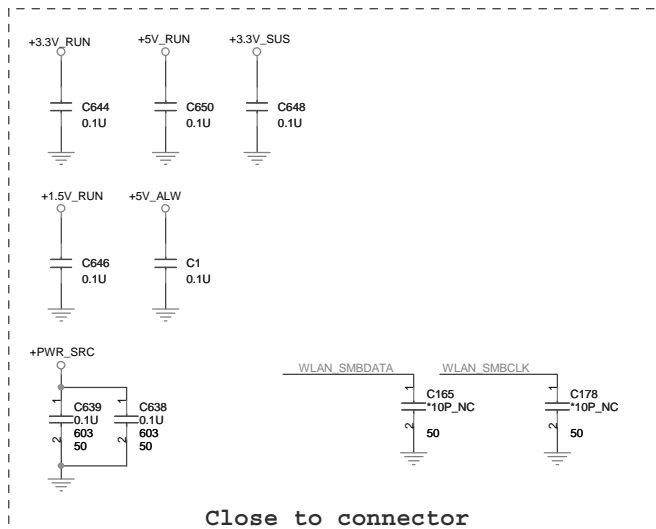
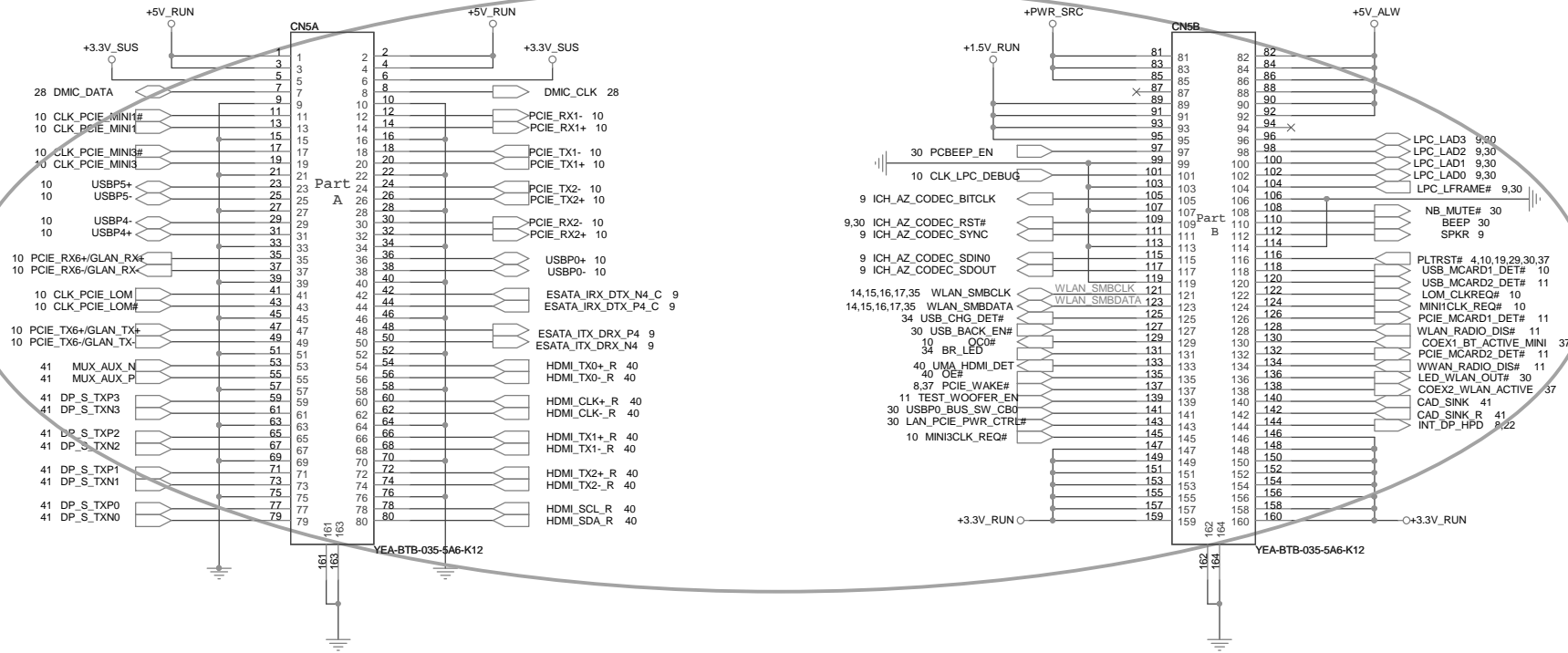
ODD Connector



Place caps close to connector.

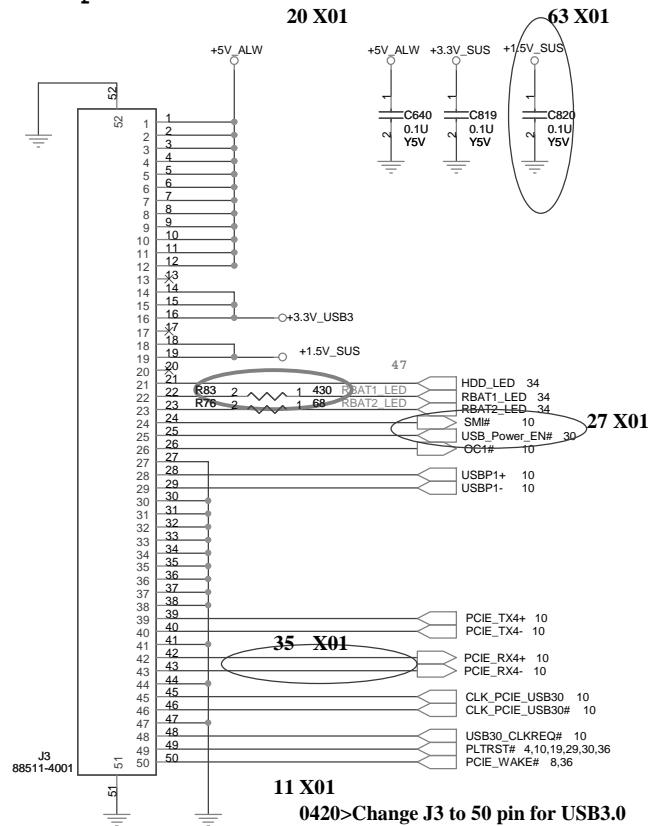


X02-11



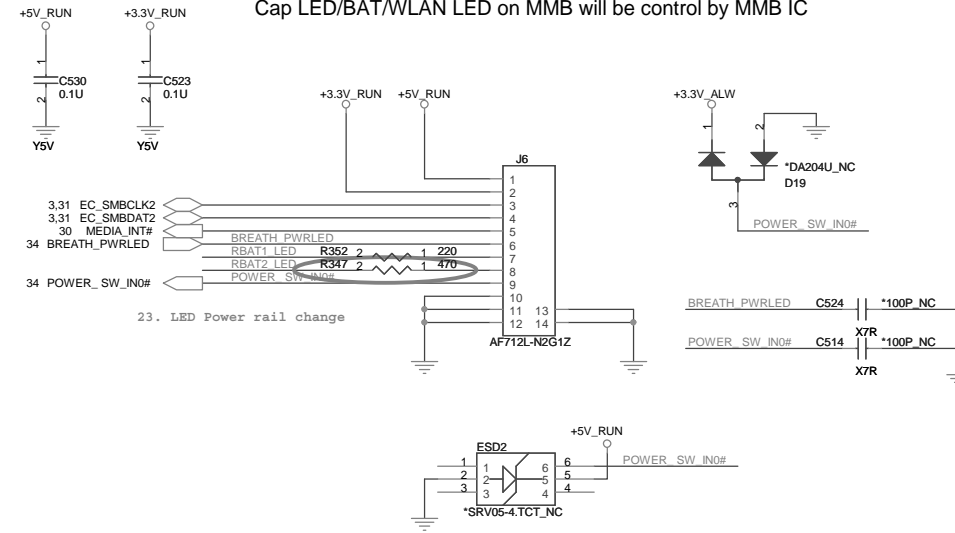
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USB IO 50 pins



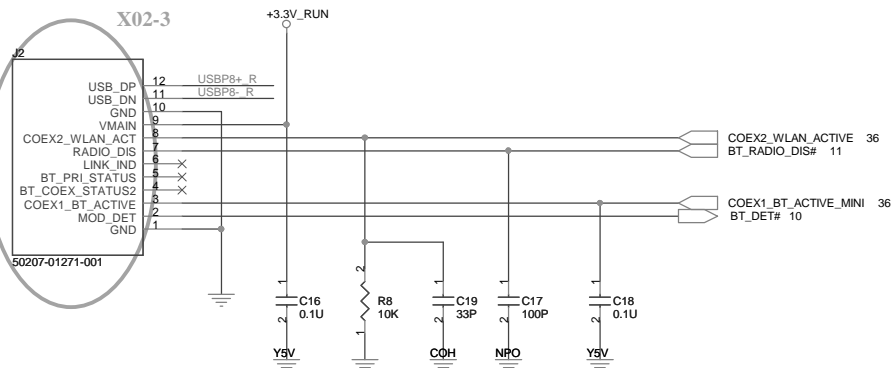
MMB & Power Board 12pins

Cap LED/BAT/WLAN LED on MMB will be control by MMB IC

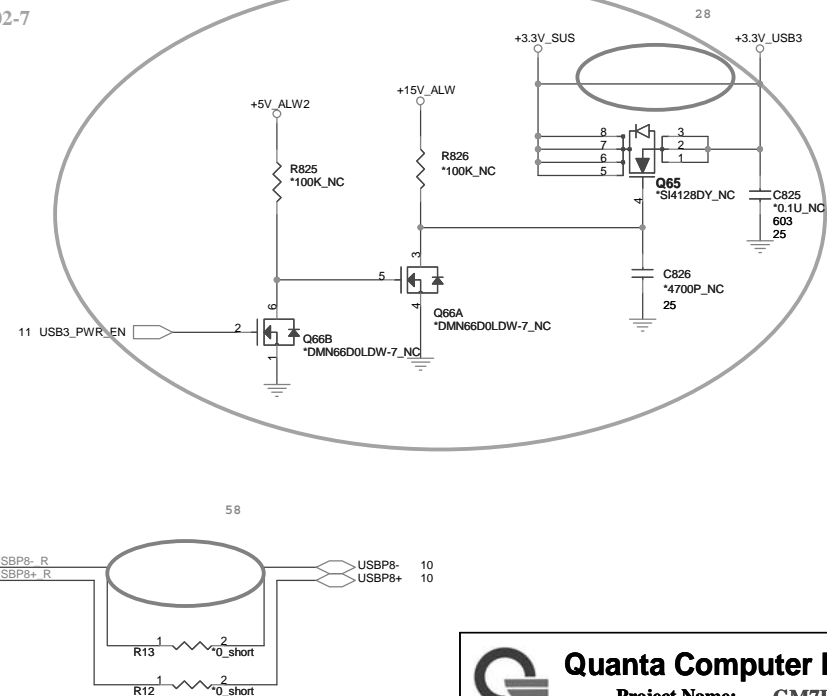


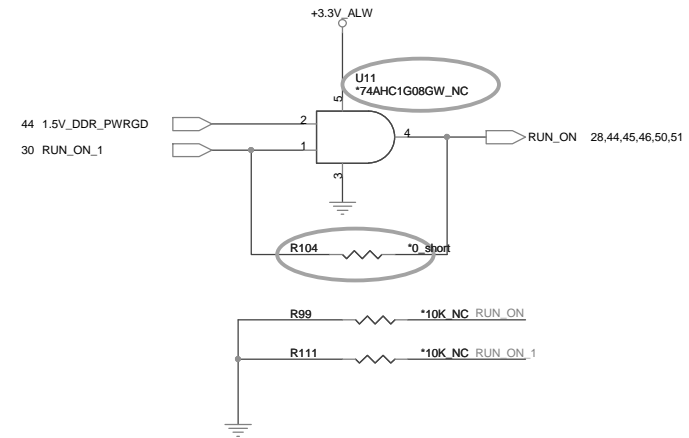
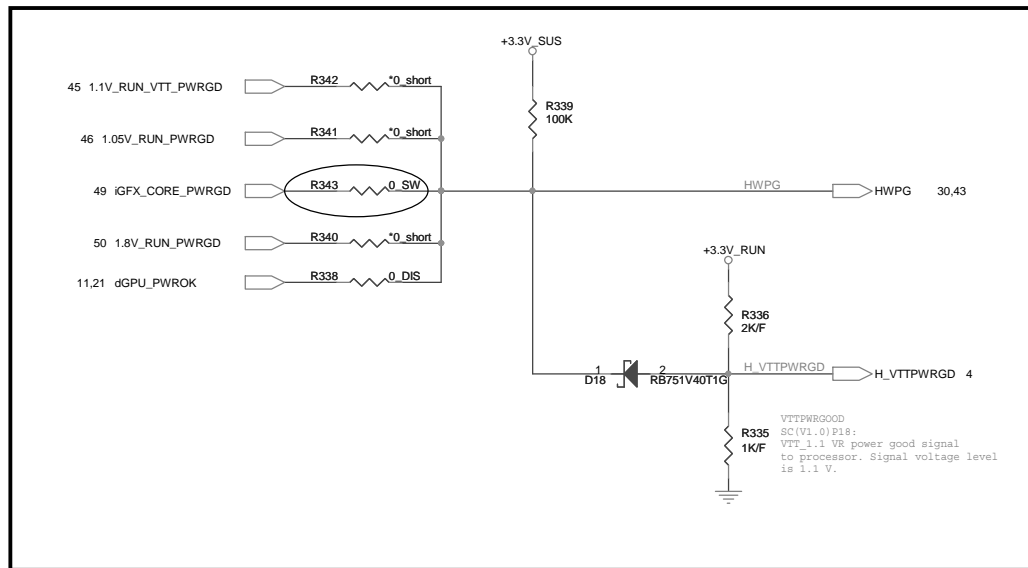
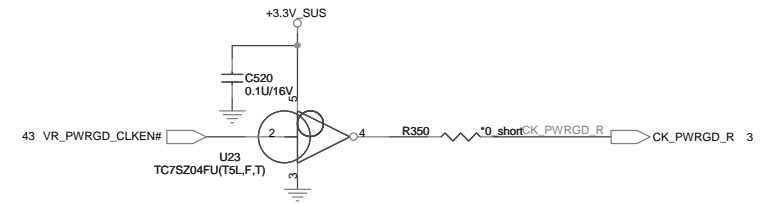
Support Dell BT375 module

Bluetooth WTB Conn

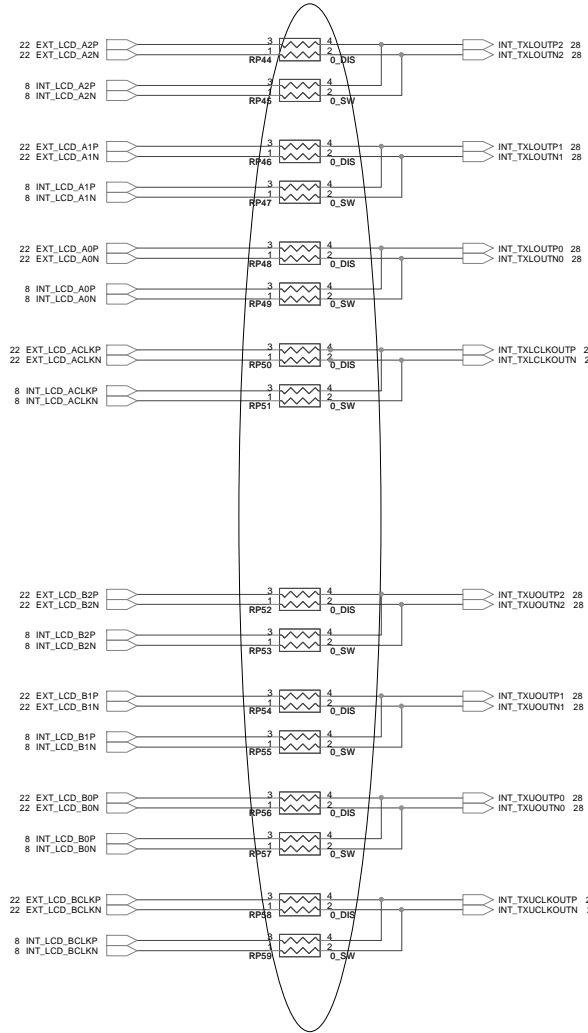


X02-7

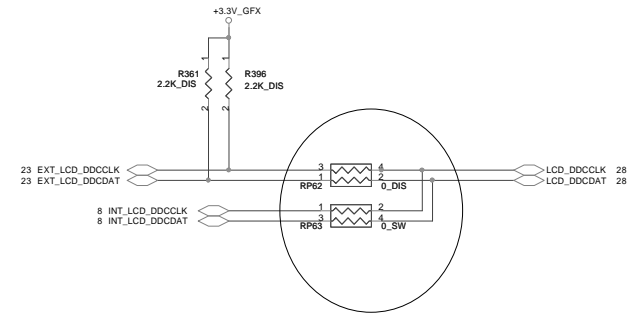





LVDS Option



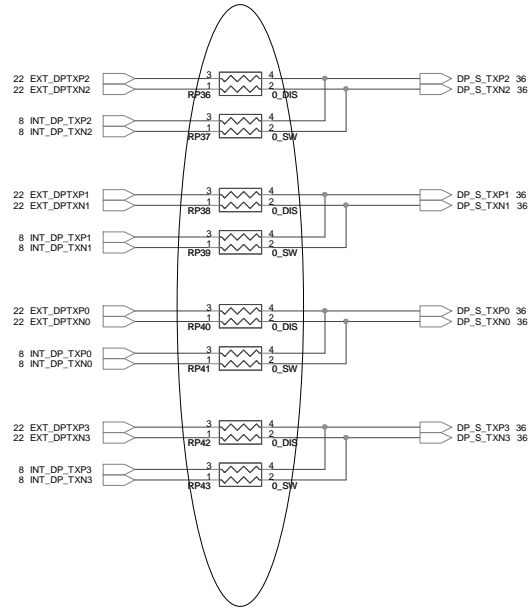
15 X01
0423>Delete MUX and add option resistor



25 X01
0503>Delete circuit for GPU_SELECT

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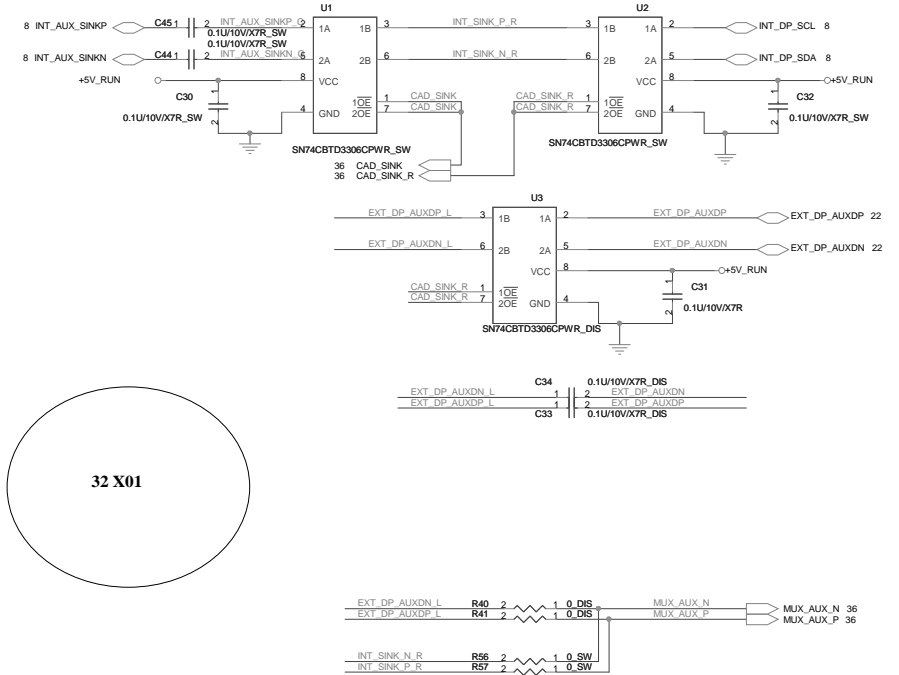
Remove Switch and use option resistor



14 X01

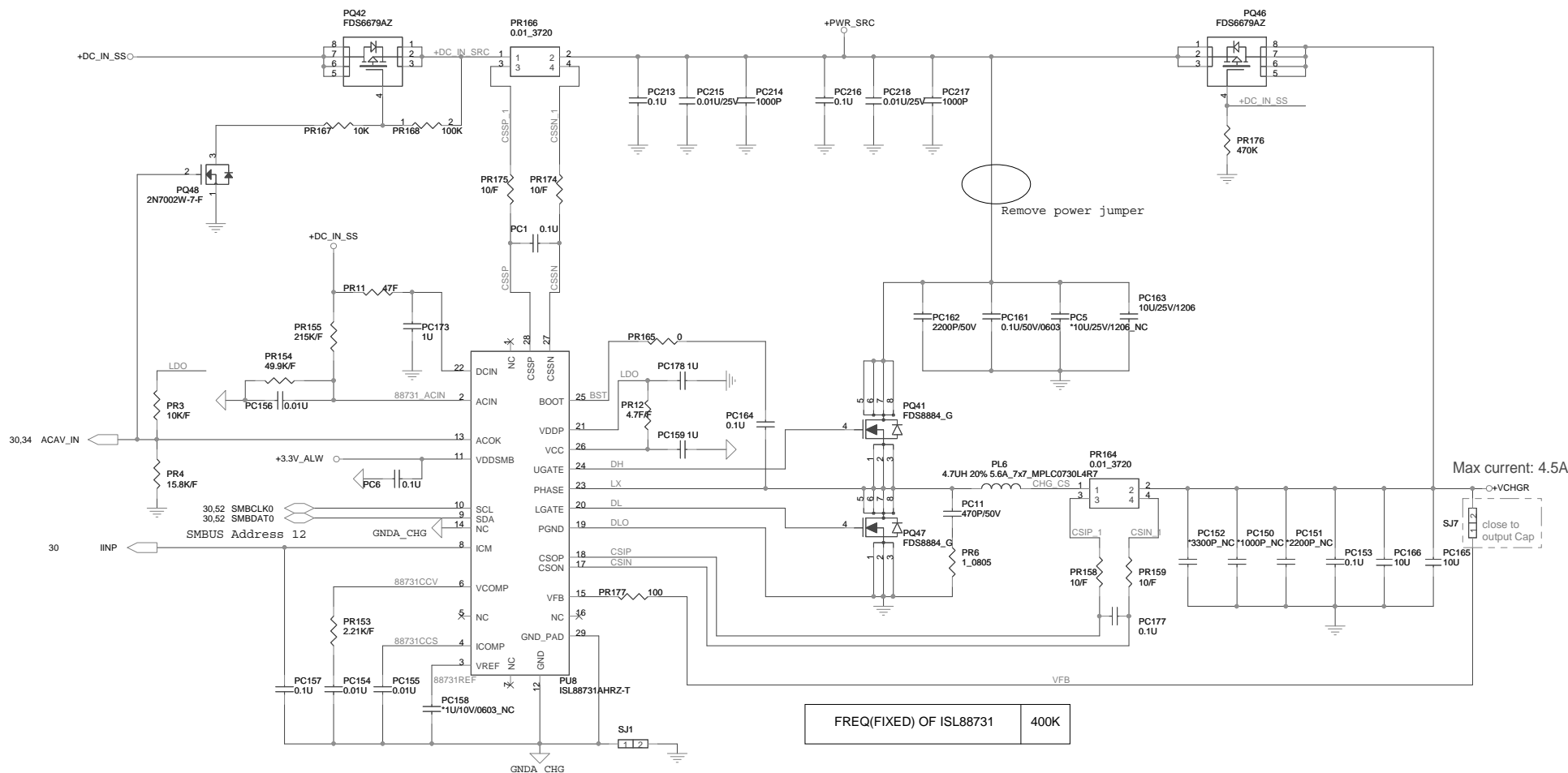
0423>Delete MUX and add option resistor

Dual Mode Support



dGPU_SELECT	Output
L	DIS only/Hybrid-DIS
H	Optimus/Hybrid-UMA

OE	Output
L	A=B
H	Z

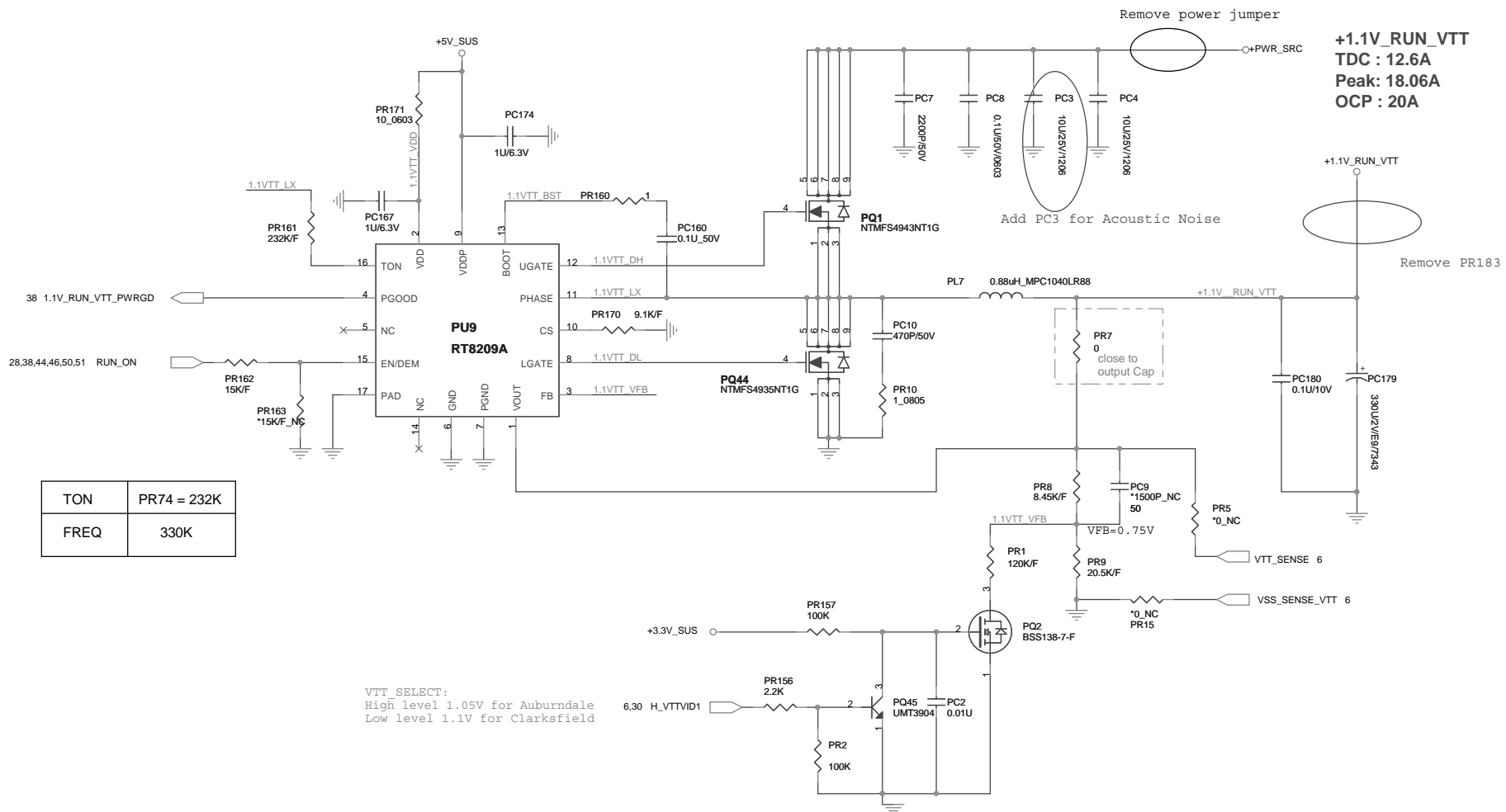


TON	PR67 = 620K
FREQ	400K

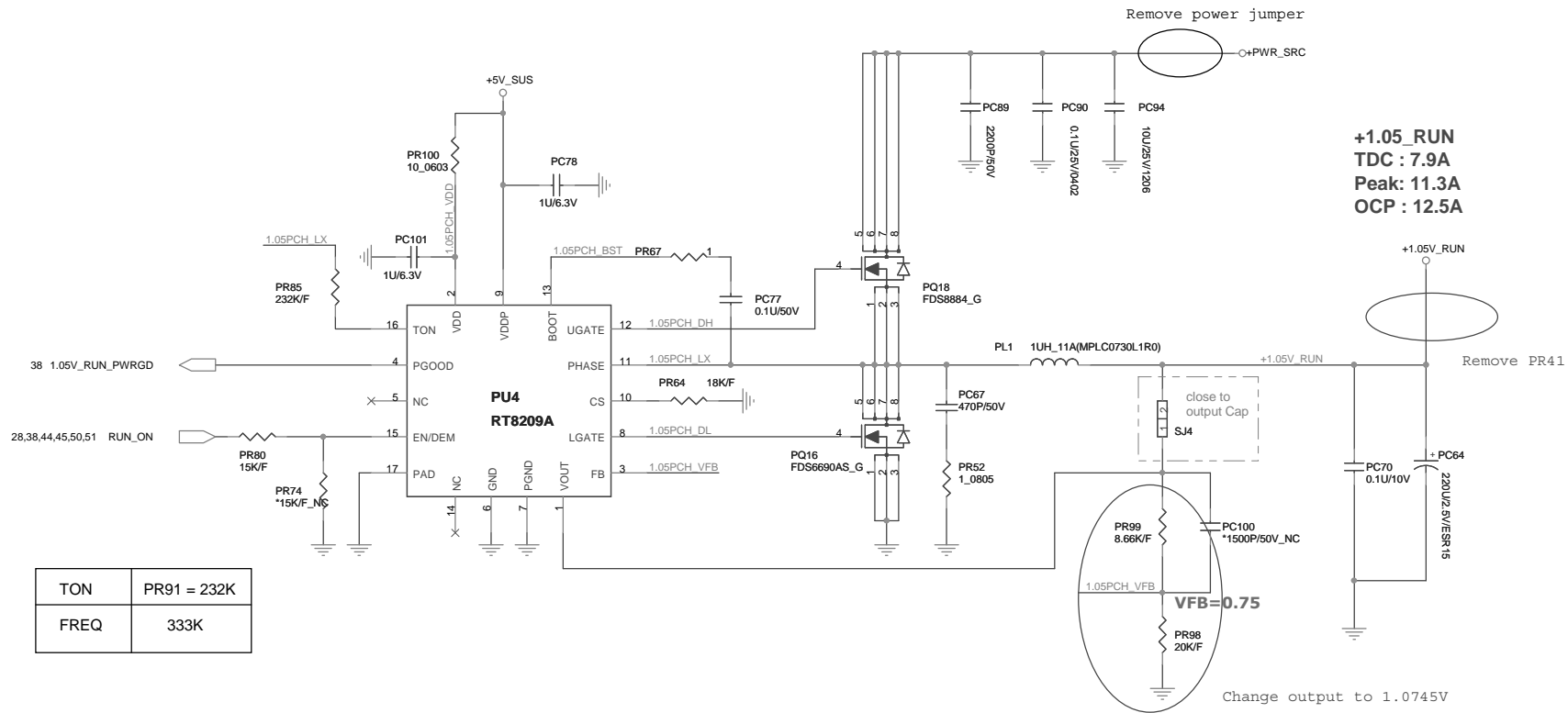
VDDQ and VTT discharge control	
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

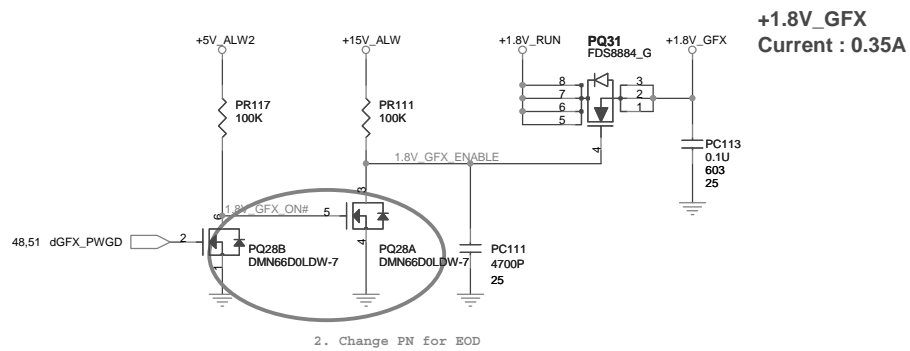
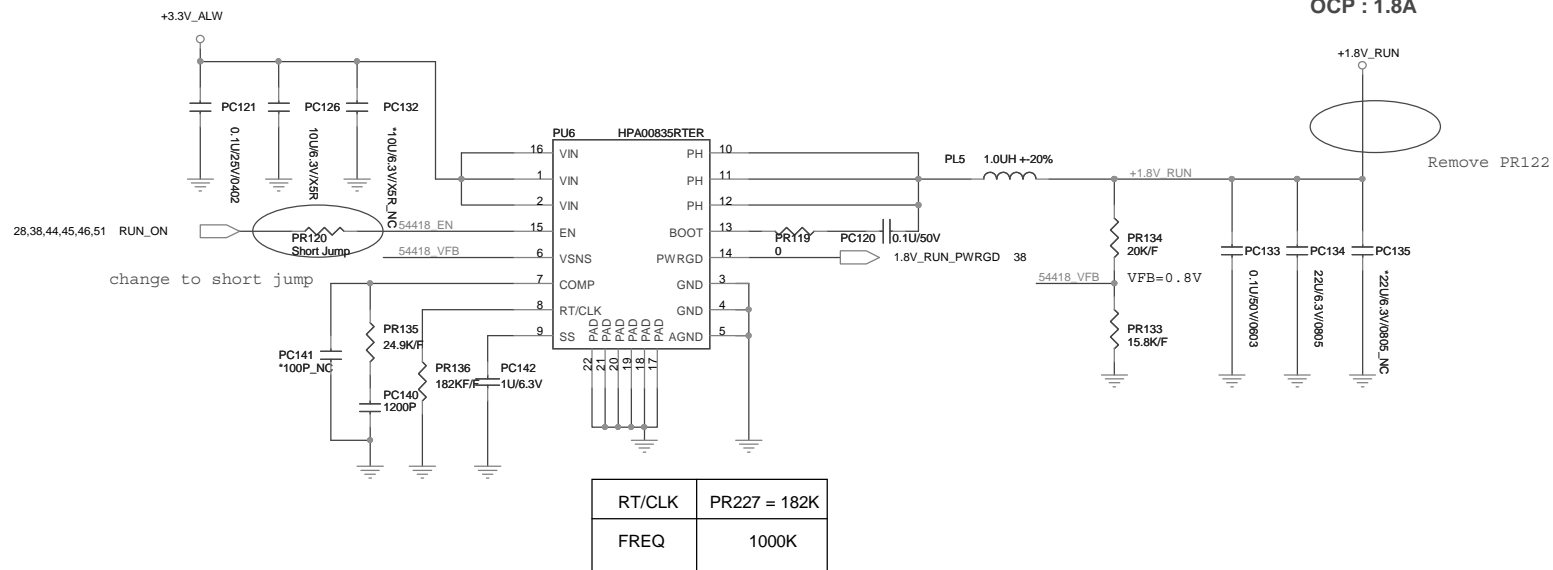
VDDQ output voltage selection			
FB	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	0.75V < VDDQ < 3.3V

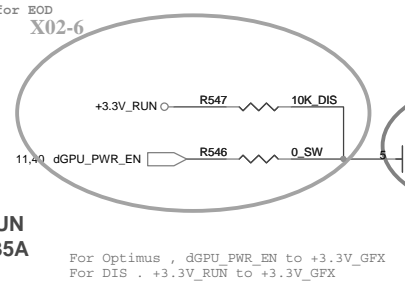
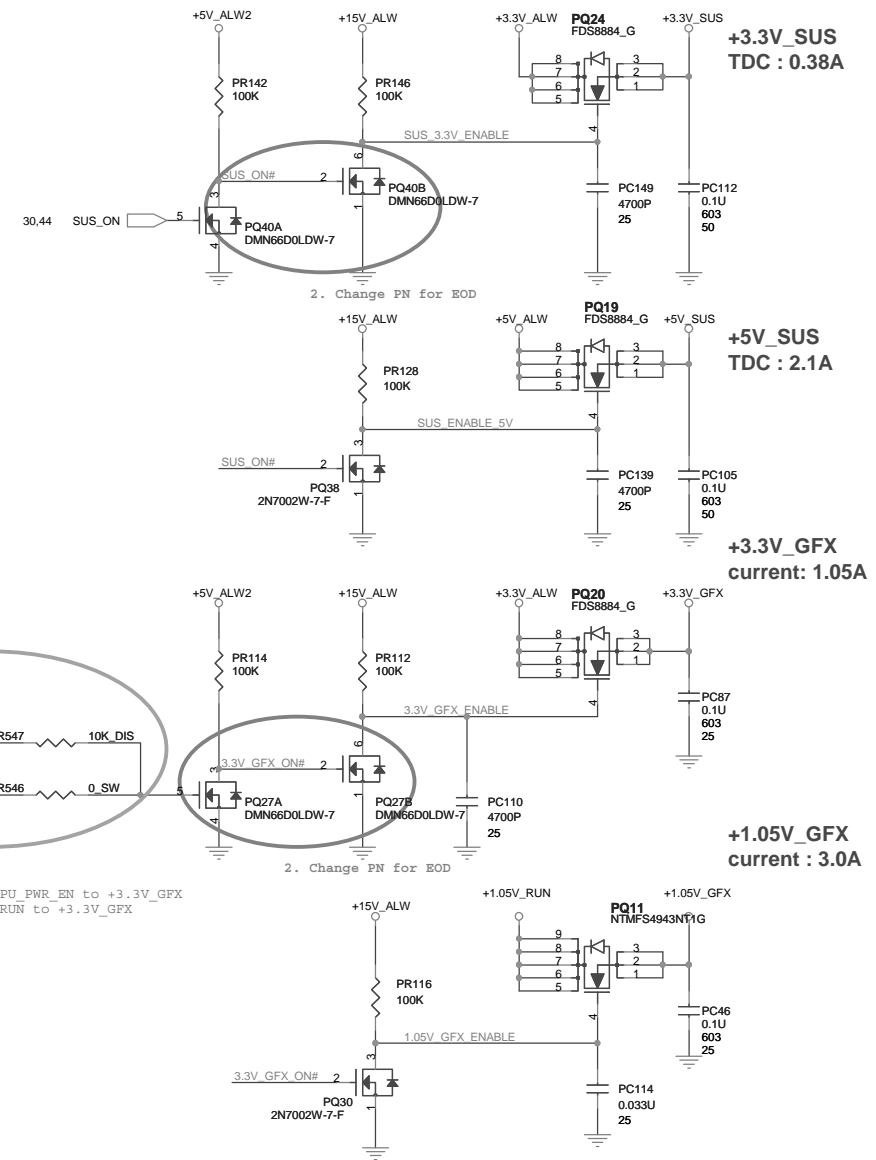
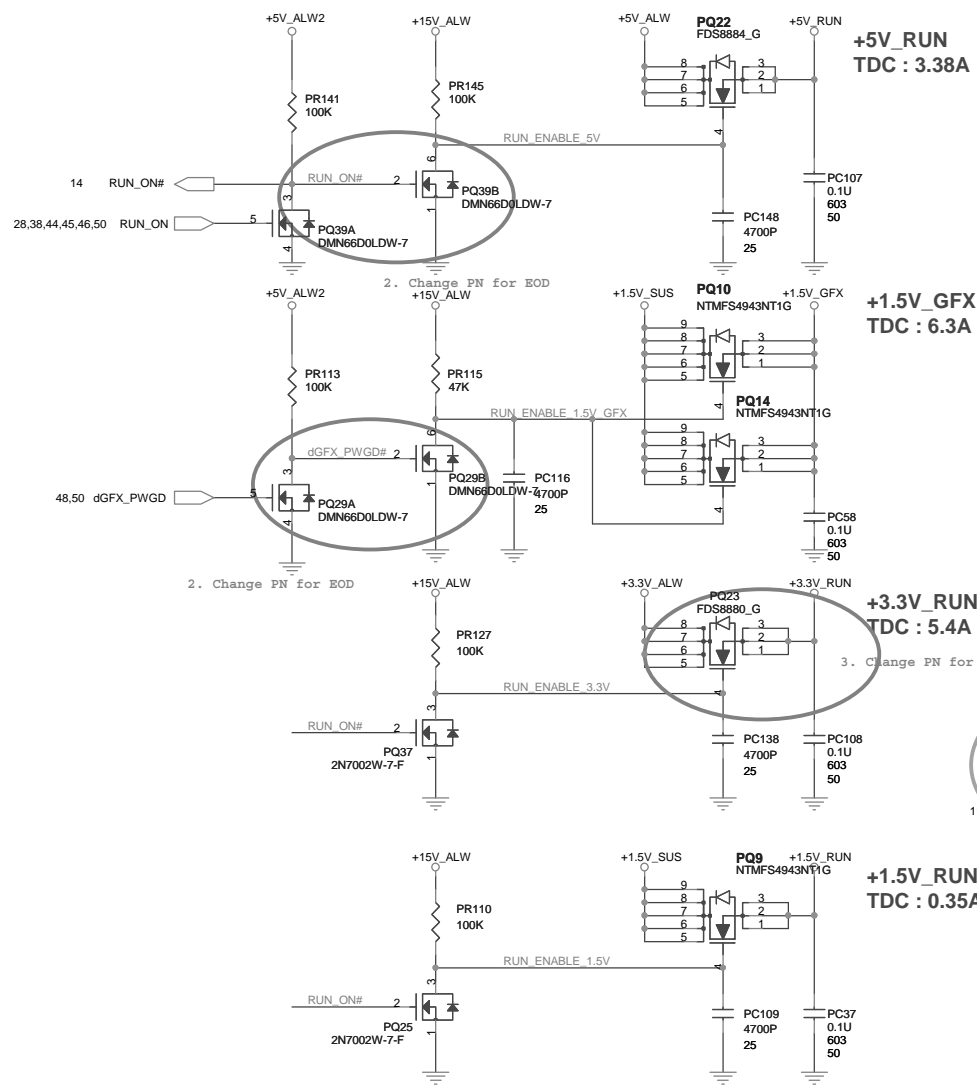
Outputs Management by S3, S5 control					
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)



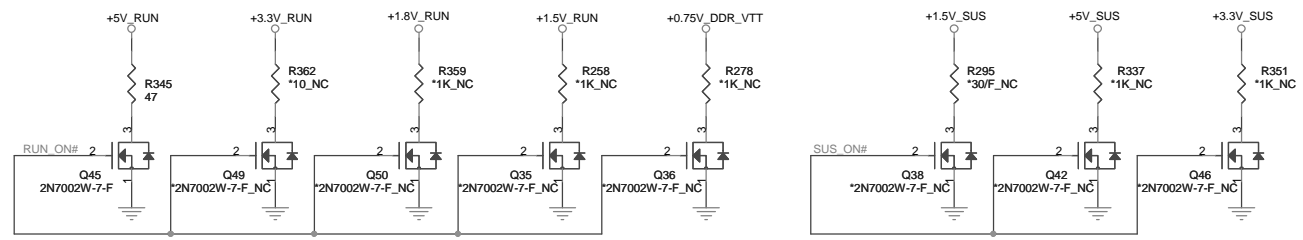
TON	PR74 = 232K
FREQ	330K

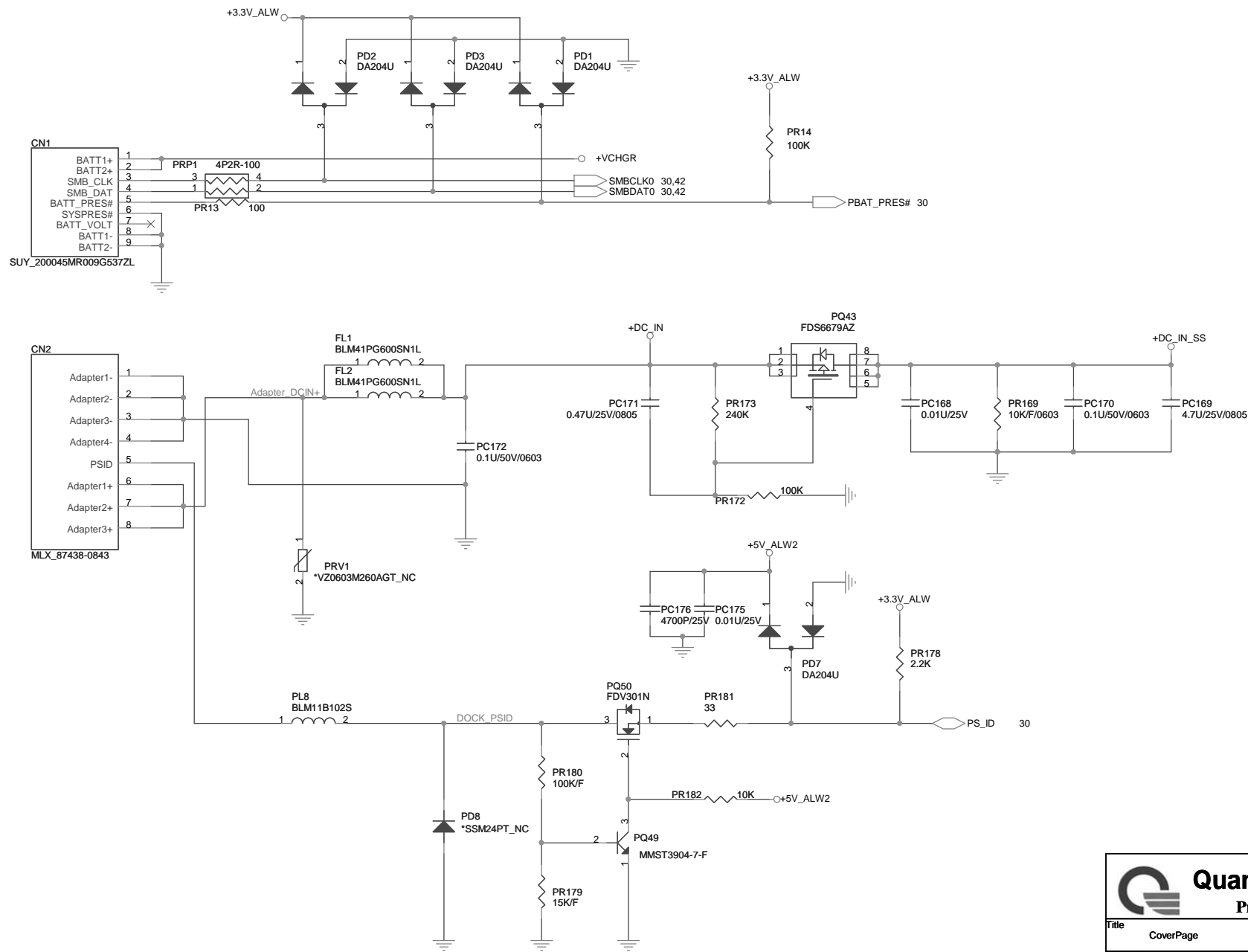


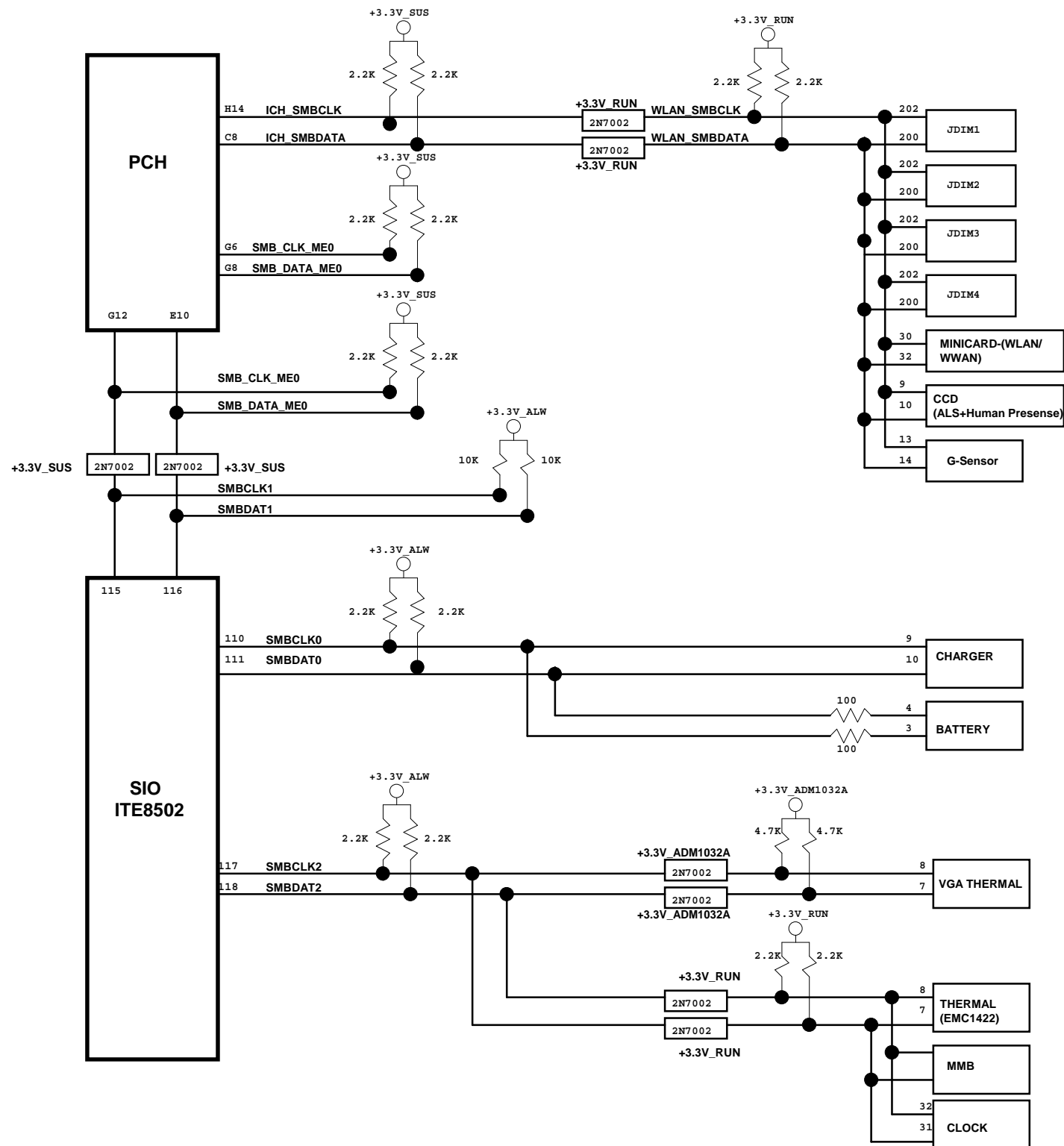




Reserve discharge path







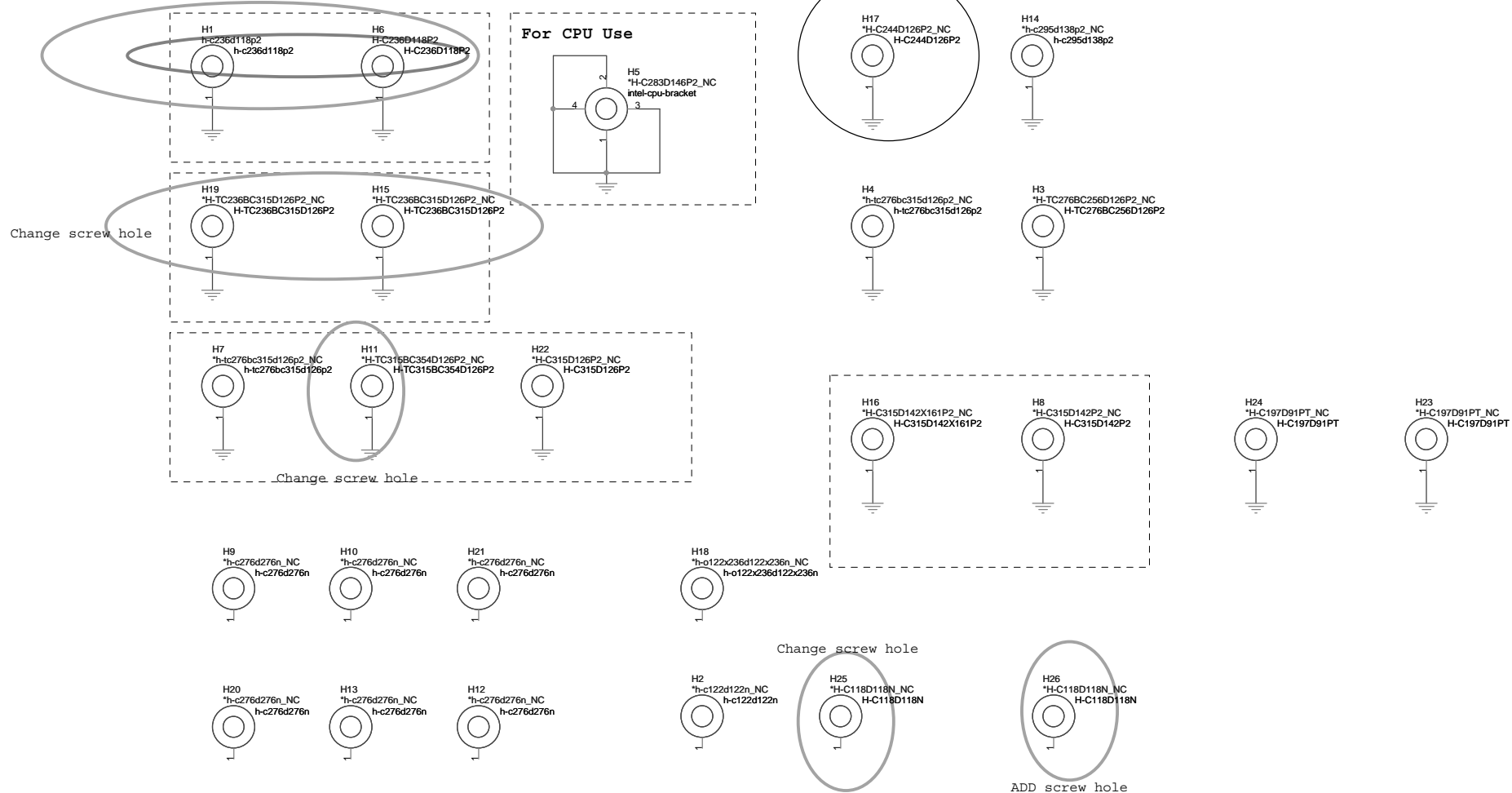



34. add label

6. layout change to BOT side

For BTB Use

For CPU Use



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